Technical Report No. 3

SPECIAL STUDIES OF AROD SYSTEM CONCEPTS AND DESIGNS

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1. INTRODUCTION AND SUMMARY

This report constitutes the Third Technical Report on the results of a program of investigations carried out by ADCOM, Inc. under Contract No. NAS8-20128 for George C. Marshall Space Flight Center, Huntsville, Alabama. The specific subject of this report is the Airborne Ranging and Orbit Determination (AROD) Ground Station Antenna and Direction-Finding System. The work on this report was conducted in close coordination with, and in direction support of, the Astrionics Division, George C. Marshall Space Flight Center.

The overall objective of the program is to investigate signaling and signal processing techniques for the AROD system that will most simply and effectively yield unambiguous range and range-rate measurements, within the limitations of existing sources of error, and in harmony with other vehicle and ground station instrumentation functions. The result of the investigations will aid NASA in the planning, design, and implementation of the AROD tracking system.

Some of the weaknesses in the original AROD ground station direction-finding (D/F) receiver design were discussed in Technical Report No. 2 of Contract No. NAS8-20128. As a result, the need for a more sophisticated D/F receiver design approach was realized and alternate designs, intended to overcome the problem areas characteristic of the original receiver, were presented in that Technical Report. The alternate designs proposed encompassed the RF section of the D/F receiver.

This report concludes ADCOM's proposed VHF direction-finding receiver design, covering the remaining sections of the receiver requiring definition: phase metering circuits, methods of selection and switching of RF signals, and generation of timing and other control signals. The RF design documented in Technical Report No. 2 has been updated and is included in this consolidated report on proposed AROD D/F receiver designs.

The following guidelines have been adhered to in the development of alternate VHF direction-finding (D/F) receiver designs:

a. The D/F receiver must function over the operating dynamic range of the AROD Station Control Receiver.

b. Alternate designs must provide for direct substitution of the new D/F receiver in the presently conceived VHF antenna system.

c. The requirement for high reliability dictates minimum circuitry consistent with required performance; circuits employed must be within the current state-of-the-art.

d. Alternate D/F receiver designs must provide for sufficient stability to maintain antenna pointing position accuracy for long periods of time without the necessity for equipment adjustments or calibration.

Various direction-finding receiver techniques are discussed in Section 2 which are intended to overcome some of the basic shortcomings of the original D/F receiver. Two fundamental receiver designs are presented, both of which utilize local oscillator signals from the Station Control Receiver for removal of doppler.

In Section 3 several methods of achieving the narrow noise bandwidth required of the D/F receiver are presented, included in which are phase-locked loops used as filters, and conventional filters. Acquisition time of phase-locked loops (including both frequency and phase lock times) is considered, as is derivation of AGC voltages. A brief survey of the various types of conventional filters considered for use in the system is included.

Phase meters with linear sawtooth characteristics are considered in Section 4 for use in the D/F receiver. The design of two such phase meters is developed: one utilizing analog integration techniques, and the other employing a type of digital integration. Noise immunity and other requirements of the phase meter zero crossing detectors is discussed.

In Section 5 the criteria and circuits for selection of RF and AGC signals is developed, as is the generation of gating signals to control their routing. Two methods for effecting antenna ring selection are presented, one involving the amplitude comparison of AGC signals from the two rings, and the other, a somewhat more involved technique, utilizing cascaded limiters with different noise bandwidths.

Timing and control signals necessary for the proper functioning of each of the D/F receiver sub-sections are discussed in Section 6. The design of a clock signal generation circuit is first presented. Functional control signals required for operation of the digital-type phase meter are next developed. Finally, the logic connections and circuitry for generation of RF routing control signals are shown.

2. DIRECTION-FINDING RECEIVER DESIGN

One of the most important considerations in the development of alternate D/F receiver designs for the AROD VHF antenna system is the dynamic range of input signals coupled to the receiver. With the establishment of the requirement that the receiver function adequately at very low input signal power, an inevitable question ensues as to whether an automatic tuning technique such as phase-lock should be employed in the receiver. In accordance with previously established guidelines, a dynamic range of -130 dBm to -60 dBm is required of the D/F receiver. Assuming the following parameters, the required noise bandwidth of the outputs of the phase meter is computed:

S_{min} = Lowest Carrier Power Expected at Input to D/F Antenna = -130.0 dBm (2.1)

N_o = System Input Noise Density (at 2000^oK) = $-165.6 \frac{dBm}{Hz}$ (2.2)

G_{ant} = Minimum D/F Antenna Gain (including a 6 dB margin allowance for antenna patterns of individual rings) = -8.0 dB (2.3)

T = D/F System Threshold, SNR = +8.0 dB (2.4)

The required noise bandwidth for satisfactory operation of the system is:

$$B_n = S_{min} - N_o + G_{ant} - T = -130.0 + 165.6 - 8.0 - 8.0 \quad (2.5)$$

$$= 19.6 \text{ dB greater than 1 Hz} = 91.2 \text{ Hz} \approx 90 \text{ Hz} \quad (2.6)$$

Because of a maximum anticipated doppler shift of ±6 kHz and the noise bandwidth requirement of Eq. (2.6), the use of phase-locked techniques for removal of doppler from the carrier appears desirable.

2.1 Channel Requirements

Since there are two "rings" in the D/F antenna proposed by Auburn University[1], a total of six channels of information is produced: a reference channel for each ring, and ℓ and m information channels for each ring. A design

compromise is possible concerning the number of channels required in the D/F receiver. By time sharing one channel in each ring between $\underline{\ell}$ and $\underline{m}$ inputs (this feature was implemented in the original D/F receiver design), the total number of D/F receiver channels required may be reduced to four.

The use of four channels allows simultaneous monitoring of signal strength in both Z and XY rings to facilitate selection of the ring ultimately to be used for directional control of the S-band antenna. Assuming that the reference channel in each ring is, indeed, a valid criterion for selection of the ring whose signals will control the S-band antenna steering, the number of channels required in the D/F receiver may be further reduced to three. A three-channel D/F receiver would require the time sharing of $\underline{\ell}$ and $\underline{m}$ signals from both Z and XY rings.

It is possible to reduce the number of channels required in the D/F receiver to two by employing all of the time-sharing techniques discussed above, plus the sequential sampling of Z and XY reference channels to determine the better ring for steering control of the S-band antenna. The use of this technique is questionable, however, because the signal quality samples thus obtained may not be as valid as continuously monitored information and usable phase measurements could be made during only a portion of the total sampling period.

At least two frequency conversions are desirable in the D/F receiver to provide adequate image rejection and avoid unnecessarily complex preselectors. Three frequency conversions may be necessary for translation of the signals to center frequencies suitable as inputs to some phase meters.

It is desirable to have the first frequency conversion in the D/F receiver occur after the attenuator and phase shifters used to normalize the four signal channel voltages in each ring, because the amount of phase shift required is easier physically to implement at the carrier frequency (138 MHz) than at some lower intermediate frequency.

2.2 Suggested Receiver Design

One receiver embodying the criteria discussed above is shown in Fig. 2.1*. The local oscillator signals e_1 and e_2 shown in this suggested design are developed in the Station Control Receiver, which has buffered outputs suitable for coupling to the VHF D/F receiver at the interfaces shown. Local oscillator signals e_1 and e_2 are nominally 96.3 MHz and 32.1 MHz, respectively. Through the use of a phase-locked carrier loop in the Station Control Receiver, these local oscillator signals contain the proper frequency shifts for complete removal of doppler from the signal at the outputs of the second IF amplifier in the proposed D/F receiver.**

Conversion of second IF outputs to a third intermediate frequency is required for most phase measurement techniques. The stable local oscillator required for this conversion may be derived by frequency division/synthesis of the reference signal e_r coupled from the Station Control Receiver. The constraints on the upper and lower bounds of the third IF design center frequency f_3 are the following: (1) the IF center frequency must be within the input frequency range of the phase meter, (2) if conventional noise filtering techniques are employed, the IF center frequency must be low enough to permit the use of filter circuits with practically realizable Q's, and (3) judicious choice of the IF center frequency must be made so that if foldover of modulation sidebands at zero frequency occurs, any resulting sideband products do not fall within the third IF passband.

Suitable local oscillator signals for all three stages of conversion could be developed within the D/F receiver by a scheme similar to that employed in the Station Control Receiver. Since these signals are conveniently available

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* On all figures in this chapter, switches (S_2, S_3, etc.) are numbered to correspond with the D/F receiver designations of References 1 and 2.

** See Appendix A.

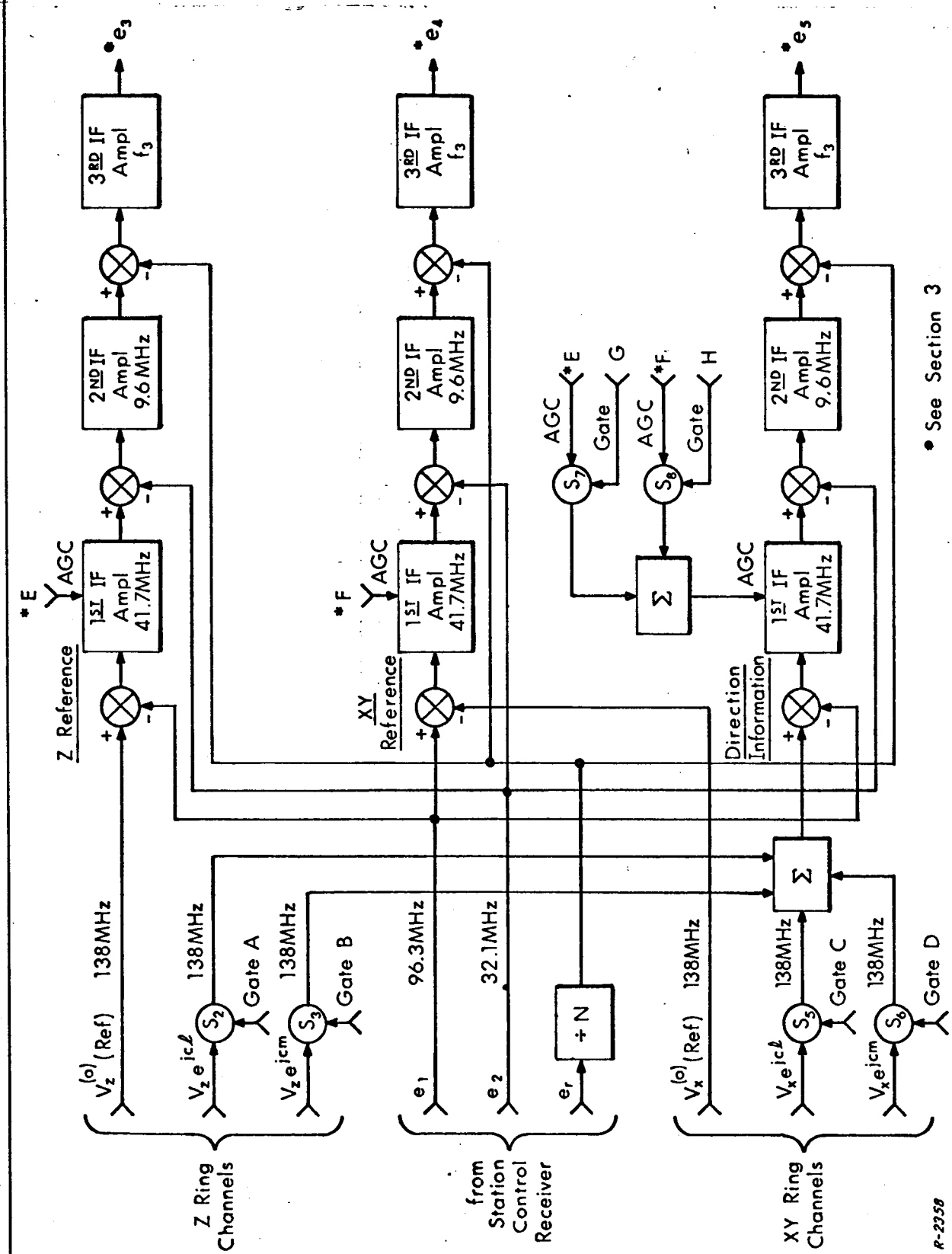

Fig. 2.1 VHF Direction-Finding Receiver.

within the Station Control Receiver, however, it is reasonable to avoid duplication of circuitry by simply coupling them to the D/F receiver. The use in the D/F receiver of the local oscillator signals developed in the Station Control Receiver requires the intermediate frequencies shown in Fig. 2.1. If, for some reason, other intermediate frequencies are desired, it would then be necessary to generate the proper signals within the D/F receiver.

Use of AGC is indicated due to the large dynamic range of input signals to the D/F receiver. AGC feedback to the first intermediate frequency amplifier – and RF amplifiers, if required – permits operation of the relatively narrowband second intermediate frequency amplifiers at constant gain. This technique enhances the phase characteristics of the receiver as a function of signal dynamics by gain control of comparatively wideband stages.

Switching of direction information signals $V_z e^{jc\ell}$, $V_z e^{jcm}$, $V_x e^{jc\ell}$, and $V_x e^{jcm}$ to the D/F receiver direction information channel is accomplished by gating signals and switches. The switching operation is sequential and periodic for ℓ and m information signals, and depends on which ring – Z or XY – provides the more reliable information for S-band antenna switching.

The development of AGC voltages and their switching, as well as signal selection criteria and the development of appropriate gating signals, will be covered in subsequent sections of this Technical Report.

The long-term phase stability characteristics of the individual channels in the D/F receiver proposed are of particular importance. Amplifier/filter phase drift must be minimized in the design suggested, since the characteristics of reference and directional information channels are independent of one another. Temperature compensation of the various stages would undoubtedly be necessary for the required stability.

2.3 Alternate Suggested Design

Another approach worthy of consideration in view of the critical channel phase differential stability requirements outlined in the previous paragraph is the one shown in Fig. 2.2. The signal inputs are switched in the same manner as in Fig. 2.1. Local oscillator signal e_1, however, is supplemented in the alternate design by local oscillator signals e_6 and e_7. As a result the Z and XY reference signals are offset in frequency at the input to the first IF amplifier by ±300 kHz, respectively, thus allowing the use of a single receiver channel for the amplification and conversion of all three signals. More important than the possible value of elimination of two entire channels of equipment, is the fact that the problem of differential phase stability is reduced to a minimum by passing all three signals through a common channel.

The bias frequency offset introduced to the two reference signals through the synthesis of local oscillator signals e_6 and e_7 is a constant. Although the center frequencies of the three signal components coupled to the second IF amplifier are staggered, complete removal of doppler from all signals is effected by utilization of local oscillator signal e_1 in the synthesis of e_6 and e_7.

Examples of the synthesis of signals e_6 and e_7 for the receiver design depicted in Fig. 2.2 are shown in Figs. 2.3a and 2.3b. Figure 2.3a shows a synthesizer which uses conventional filters. Care must be taken in the design and construction of filters, if this technique is used, so that the phase of the reference signal carriers is not altered as a function of temperature and doppler frequency changes. e_9 and e_{10} are synthesized by mixing e_r and frequencies derived from e'_r. e_r, e_9, and e_{10} are used as third local oscillator signals (see Fig. 3.4).

Phase-locked loops may also be used as filters in the synthesis of local oscillator signals e_6 and e_7, as shown in Fig. 2.3b. Among other factors, the frequency dynamics of e_1 as contributes to the loop phase error must be considered, since this error affects the directional steering accuracy of the overall antenna system.

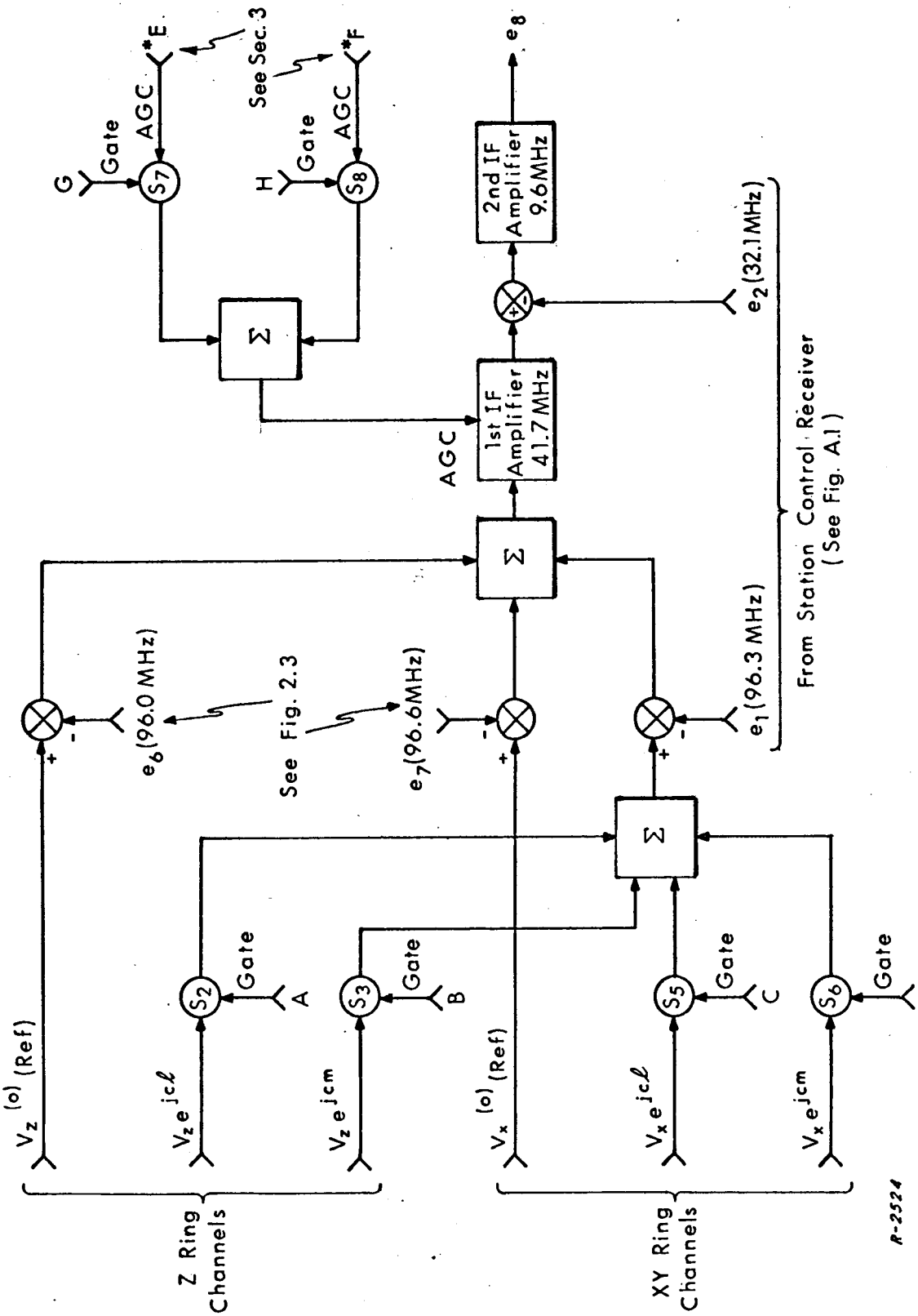

Fig. 2.2 Alternate Design VHF Direction-Finding Receiver.

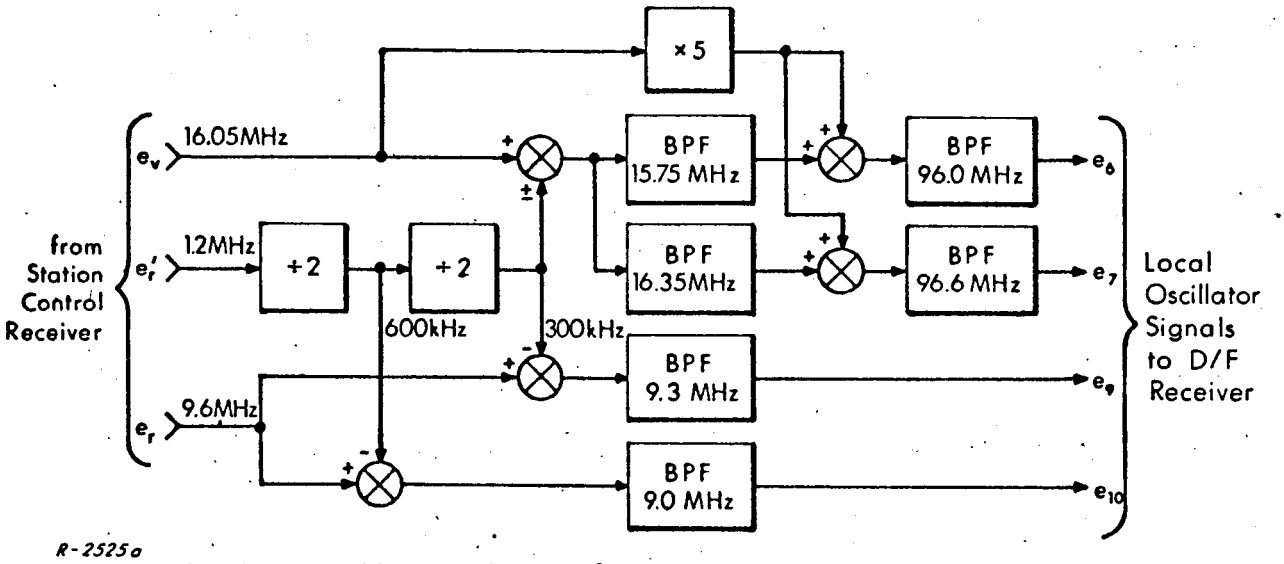

Fig. 2.3a Frequency Synthesizer Using Conventional Filtering.

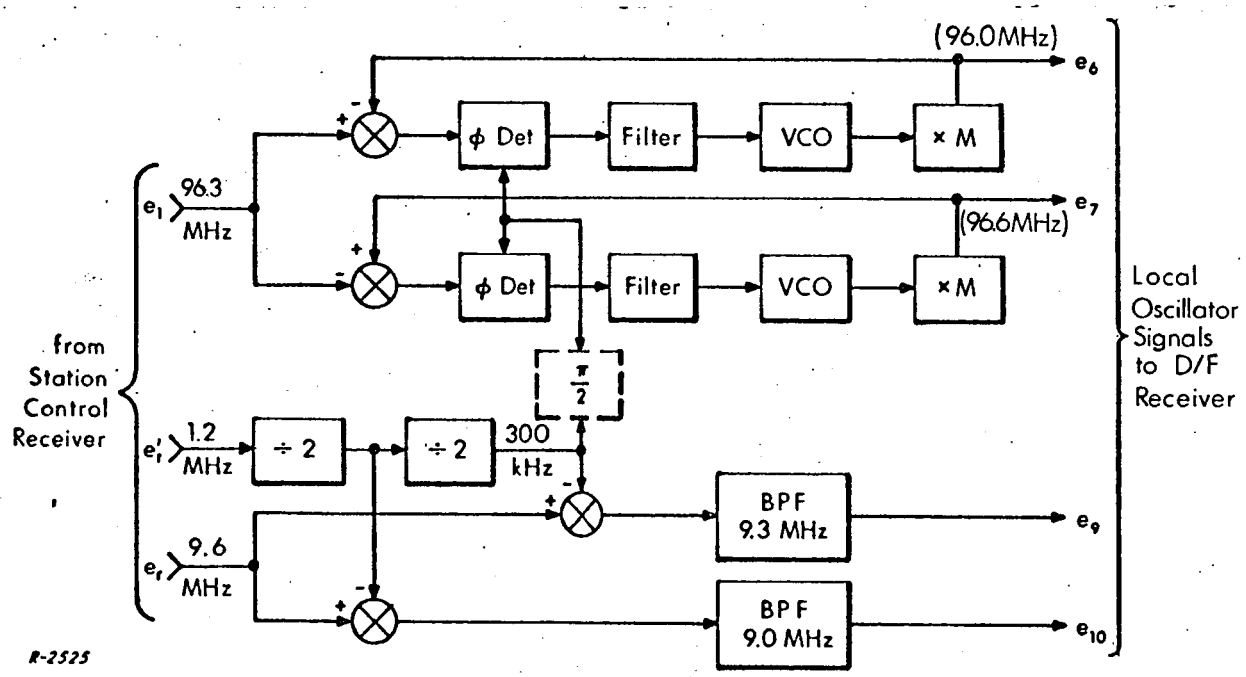

Fig. 2.3b Frequency Synthesizer Using Phase-Locked Filtering.

3. NOISE BANDWIDTH CONSIDERATIONS

Several methods are possible for achieving the 90 Hz noise bandwidth required of the D/F receiver. Two types of filtering techniques are discussed below, one involving the use of phase-locked loops (PLL's), and the other utilizing conventional filters.

3.1 Phase-Locked Loop as a Filter

By employing the phase-locked loop as a filter, the noise bandwidth requirement of Eq. (2.6) may readily be achieved. In the method depicted in Fig. 3.1, outputs from the third IF amplifier in the D/F receiver of Fig. 2.1 are coupled to the PLL's. The net effect of utilizing the carrier tracking loop in the Station Control Receiver to provide the first and second local oscillator signals for the D/F receiver is that there are no carrier frequency dynamics for the filtering PLL's to track out. This technique allows the loops to operate at noise bandwidths much less than 90 Hz to reduce the noise on the signals coupled to the phase meter. In addition, the narrower bandwidths might allow RF amplifiers to be eliminated from the system with a consequent increase in system noise figure. The advantages of elimination of RF preamplifiers are the following: (1) the problem of obtaining the required differential phase stability between channels is greatly reduced if no RF preamplifiers are required and the receiver design shown in Fig. 2.2 is implemented, and (2) standby primary power requirements are greatly reduced.

Prior to PLL acquisition, any frequency difference between the output signal of the third IF amplifiers (e_3, e_4, or e_5) and the rest frequency of the corresponding loop VCO, will be caused primarily by drift in the VCO. Assuming a worst-case frequency instability of five parts in 10^5 in a passively temperature compensated 100 kHz VCO, the frequency uncertainty in the loop is 5 Hz. The acquisition time may be approximated for a critically damped loop ($\zeta = \frac{1}{\sqrt{2}}$) as follows:

$$t_f \approx \frac{33.5\,(\Delta f)^2}{B_n^3} \qquad (3.1)$$

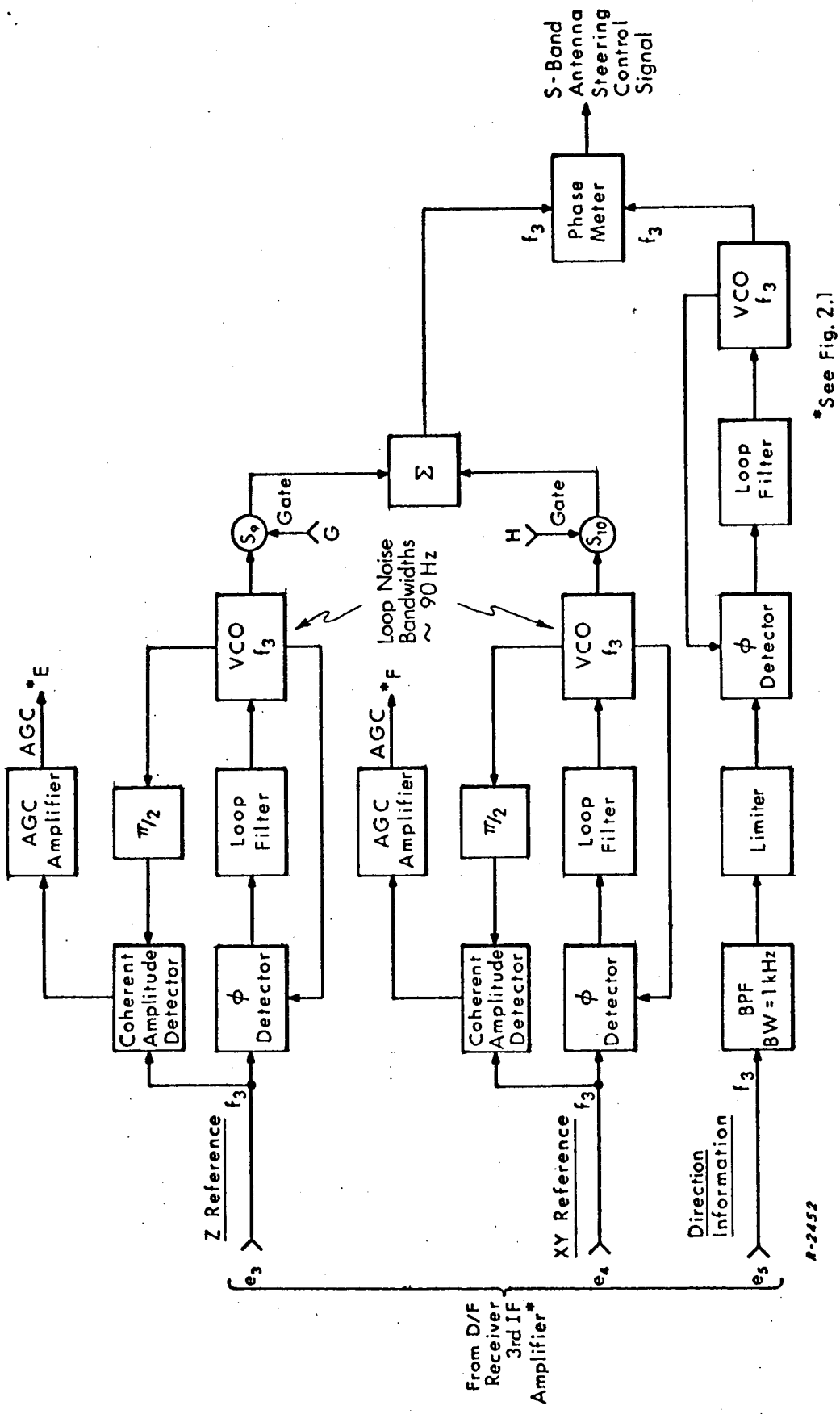

Fig. 3.1 PLL Filtering for 3-Channel D/F Receiver.

where t_f = approximate frequency lock time, seconds; Δf = frequency uncertainty, Hz; and B_n = two-sided noise bandwidth, Hz. Thus, for a 90 Hz noise bandwidth:

$$t_f \approx 1.1 \text{ milliseconds} \tag{3.2}$$

For a 30 Hz noise bandwidth:

$$t_f \approx 31 \text{ milliseconds} \tag{3.3}$$

In addition to the time required for frequency acquisition of the PLL, the time for phase transient errors to subside must be considered. Normalization of experimental data obtained by ADCOM* indicates the phase acquisition time t_ϕ for this loop to be on the order of 0.3 milliseconds. The total lock time t_L is:

$$t_L = t_f + t_\phi \tag{3.4}$$

which may be approximated to:

$$t_L \approx t_f \tag{3.5}$$

for $t_f >> t_\phi$. Thus, $t_L \approx 1.4$ milliseconds for a loop with $B_n = 90$ Hz.

Of considerably more importance than the ability of PLL's to track any slowly changing frequency dynamics in the input signal is their ability to reacquire each time the input signal changes. Since $\underline{\ell}$ and $\underline{m}$ signals are periodically time shared in the D/F receiver direction information channel, the PLL in that channel must reacquire each time the input signal is switched from $\underline{\ell}$ to $\underline{m}$ information and again when the signal changes back from $\underline{m}$ to $\underline{\ell}$ information. The loop must also reacquire each time steering information is selected from a different ring. If the switchover of input signals is instantaneous, the VCO will not return to its rest frequency, but will remain at the frequency common to the two input signals. Thus, t_L will be equal to t_ϕ. Acquisition time (t_L) of the

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* Boardman, C.J. and Filippi, C.A., "Sawtooth PLL Acquisition Experiments," ADCOM Report No. 566-RR-49, 1965.

loop under this condition will probably be less than one millisecond, since the input signal switchover time can be made to be virtually instantaneous. The loop acquisition times calculated are small compared to $\underline{\ell}$ and $\underline{m}$ sequence and information sampling periods.

Coherent AGC systems are convenient byproducts of the use of PLL's as shown in Fig. 3.1. Whenever the selection of direction information is changed from Z to XY rings, or vice-versa, there will be a period concurrent with PLL reacquisition during which IF amplifier gain transients will occur due to the switching of AGC and input signals. Since such switching times are virtually instantaneous and the IF amplifier is relatively wideband, any resulting gain transient period would probably be negligible.

The AGC input controlling the gain of the Direction Information channel first IF amplifier* is switched between AGC voltages E and F from the two reference channels.** e_3 and e_4 are thus held constant by AGC systems in their respective channels. e_5, however, will vary in amplitude as a function of the direction from which the transmitting source is radiating. Since the noise bandwidth of the PLL in the direction information channel would also vary as a function of this input signal level, a narrowband limiter is employed prior to the PLL to normalize the input signal amplitude, and thus hold the noise bandwidth fairly constant. The bandpass filter in front of the limiter will keep the signal-to-noise ratio at the input to the limiter within acceptable limits. A 1 kHz bandwidth filter will provide an approximate -2 dB minimum SNR at the Direction Information channel PLL input.

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* See Fig. 2.1.

** Operation of direction information and reference channels at equal gain is desirable to eliminate phase differentials between the two channels which might occur if separate AGC sources, and therefore separate IF amplifier gains, were employed. See Fig. 3.1 for derivation of AGC voltages.

Gating signals G and H switch the reference signal from either the Z ring channel or the XY ring channel to the phase meter, where the phase of the appropriate direction information signal with respect to the reference is measured for directional control of the S-band antenna. Development of these gating signals, as well as phase metering techniques, are discussed in subsequent sections of this Technical Report.

Three phase-locked loops may be used to filter the frequency-staggered carriers of the receiver design of Fig. 2.2 in the manner shown in Fig. 3.2. Each of the loops is phase-locked to a different carrier component coupled from the second IF amplifier. The outputs of the loops are then translated to a common center frequency (300 kHz in the example) by mixing them with e_r, e_9, and e_{10}, the latter two being local oscillator signals derived from the Station Control Receiver reference oscillator (see Figs. 2.3a and 2.3b). Limiting in the direction information channel, development of AGC signals, and reference channel switching are as in Fig. 3.1.

3.2 Conventional Filters

Conventional filtering techniques may also be used to achieve the desired noise bandwidth. Figure 3.3 illustrates the method by which this may be accomplished. Outputs e_3, e_4, and e_5* are coupled from the third IF amplifiers of Z ring reference, XY ring reference, and direction information channels, respectively, to the bandpass filters. The 90 Hz noise bandwidth requirement of Eq. (2.6) necessitates that f_3 be a relatively low frequency in order that $\frac{f_3}{90}$ fall within the range of Q's possible in practical conventional filters. Noncoherent AGC detection is provided following the filters as shown in the figure.

The use of conventional filters for filtering of the carriers resulting from the circuit of Fig. 2.2 is shown in Fig. 3.4. Adjustment of the frequency of synthesized signals e_9 and e_{10}, and of the frequency scaling factors of e_v and e'_r (see Figs. 2.3a and 2.3b), is necessary in order to achieve the three 150 kHz

* See Fig. 2.1.

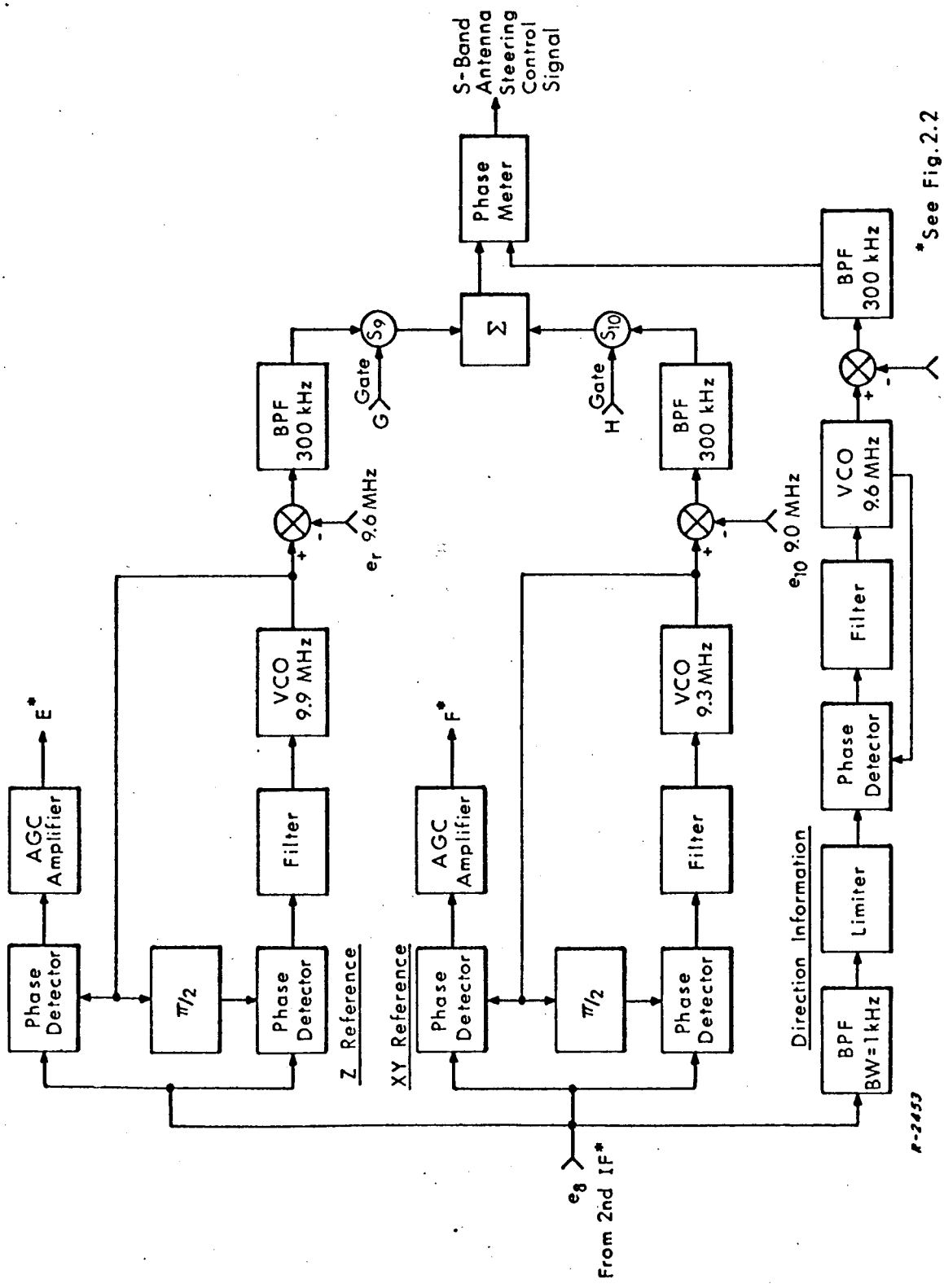

Fig. 3.2 PLL Filtering for Alternate Design D/F Receiver.

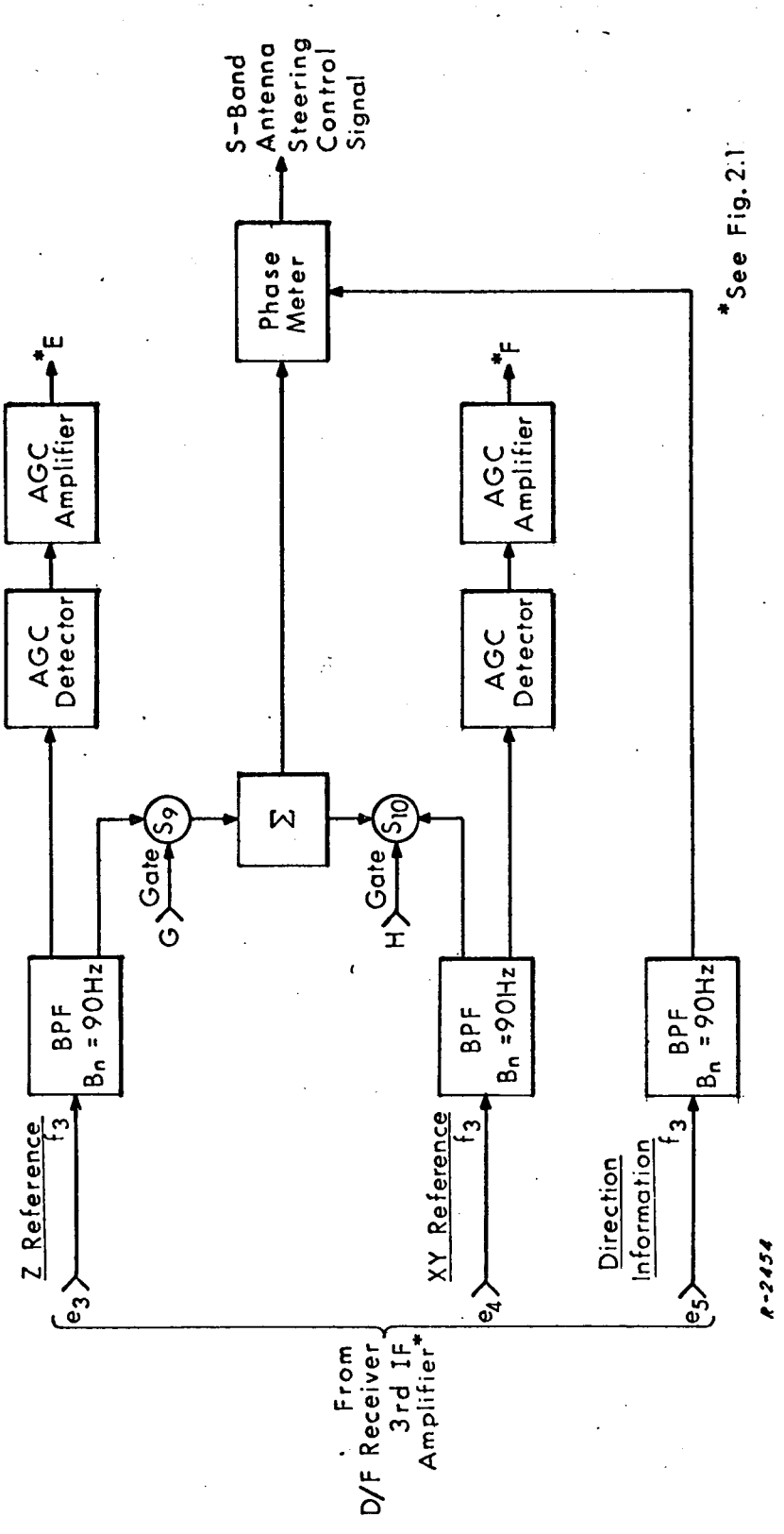

Fig. 3.3 Conventional Filtering for 3-Channel D/F Receiver.

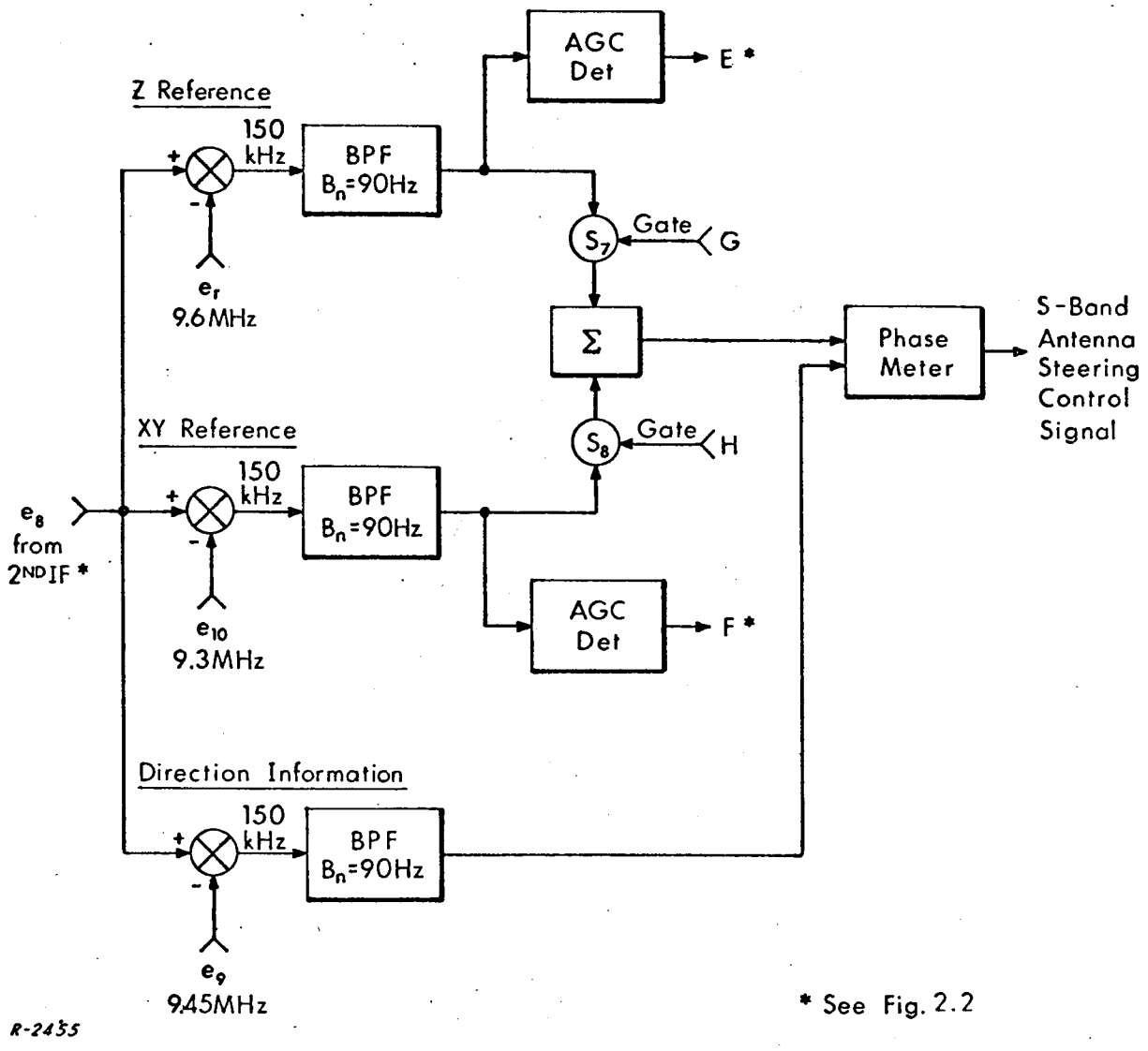

Fig. 3.4 Conventional BP Filtering for Alternate Design D/F Receiver.

carriers at the inputs to the bandpass filters. The constraint on the upper bound of this input carrier frequency is that it must be sufficiently low to accommodate the use of filters with practically realizable Q's. Assuming utilization of the conventional filter method of local oscillator synthesis,* the lower bound is dependent on the frequency separation possible between e_r and e_6, and between e_r and e_7, without phase distortion of e_6 and e_7 due to changes in doppler.

Four types of conventional filters are surveyed briefly below for the purpose of possible use in the circuits of Figs. 3.3 and 3.4:

a. Passive LC Filter: Q's of up to 20-30 are possible, meaning an upper bound carrier frequency f_3 of approximately 2.7 kHz would be required for use in the circuit of Fig. 3.3. Passive temperature compensation would be required for the desired phase and frequency stability. Passive filters could not be used in the circuit of Fig. 3.4 because of the high-Q filter requirement.

b. Active RC Filters: Q's of up to 50-100 are possible, meaning an upper bound carrier frequency f_3 of approximately 9 kHz would be required for use in the circuit of Fig. 3.3. Passive temperature compensation would probably be required for the desired phase and frequency stability. Active RC filters could not be used in the circuit of Fig. 3.4 because of the high-Q filter requirement.

c. Mechanical Filters: Q's of up to 10-1000 are possible. Center frequency may be held to within 2 parts per million per degree C over a range of -25°C to +85°C, meaning a ±17 Hz center frequency shift may occur in a filter with 75 kHz center frequency over the temperature range. Although no phase stability specifications are available for mechanical filters, available frequency stability specifications suggest that active temperature compensation might be required for the desired phase stability. The use of mechanical filters is marginal for the circuit of Fig. 3.4, but if the carrier frequency could be reduced to 75 kHz, they could be used.

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* See Fig. 2.3a.

d. Crystal Filters: Q's of up to 120-2000 are commercially available. A 90 Hz noise bandwidth means a center frequency as high as 180 kHz could be used. Active temperature compensation would be required if needed for the desired phase and frequency stability. Crystal filters could be used in either the circuit of Fig. 3.3 or 3.4.

4. PHASE MEASUREMENT TECHNIQUES

The input signals to the "phase meter" referred to in Figs. 3.1 through 3.4 consist of a reference signal and the signal whose phase with respect to the reference is to be measured. The phase meter output ultimately controls the steering of the S-band antennas.

Phase measuring circuits with linear characteristics are appropriate for the D/F receiver under consideration. Two types of phase meters are discussed in this section, both with linear sawtooth characteristics. The first presented provides an analog output suitable for coupling directly to the Auburn University analog-to-digital (A/D) Converter. The other provides digital outputs for coupling directly to the Auburn University Combinational Switching Network. The second method eliminates the need for intermediate analog processing of directional information, and may therefore be more stable over long periods of time and widely varying ambient temperatures.

4.1 Phase Meter With Analog Output

In the circuit of Fig. 4.1, outputs from Reference and Direction Information Channels are coupled to positive zero crossing detectors. Each positive zero crossing from the reference signal gates the b-stable multivibrator ON, and each positive zero crossing from the direction information signal gates the bi-stable multivibrator OFF. Since alternately there is one positive zero crossing in each input frequency cycle for each of the input signals, a rectangular wave is generated in the b-stable multivibrator whose period is that of one input frequency cycle. It is then necessary only to integrate this rectangular wave with a lowpass filter to derive an analog signal whose dc level is directly proportional to the phase difference ψ between the input signals.

The inputs and outputs to the two integrating lowpass filters shown following the bi-stable multivibrator are switched synchronously with the input

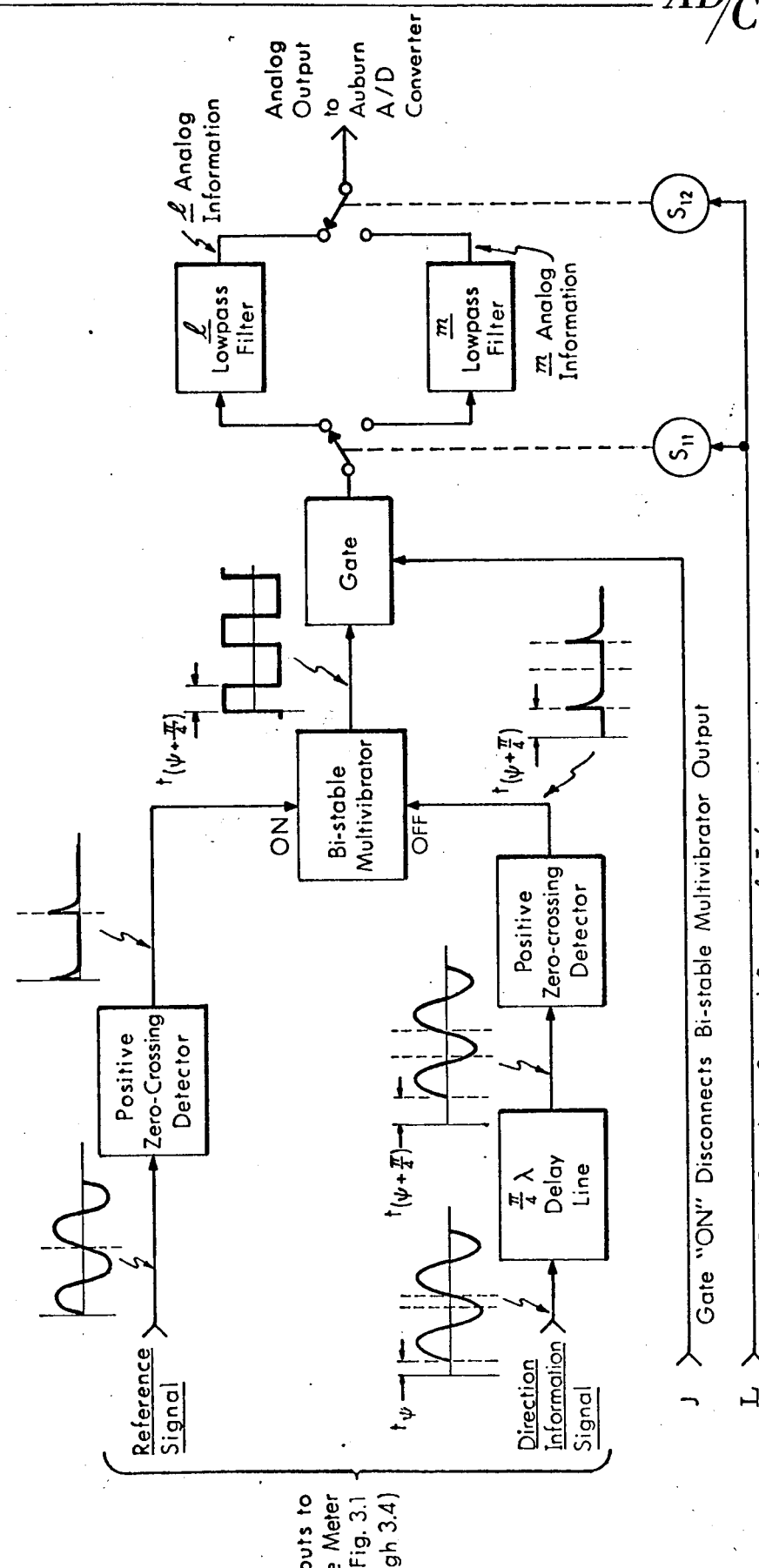

Fig. 4.1 Phase Meter With Analog Output.

to the D/F receiver direction information channel. Switching signal L* is the control signal, and the switching occurs in such a manner that analog storage of $\underline{\ell}$ information is effected in one lowpass filter and $\underline{m}$ information in the other. This switching technique and the constraints on the filter time constants are covered in detail in Appendix B. Signal J, developed in Sec. 5, causes a gate to inhibit inputs to $\underline{\ell}$ and $\underline{m}$ lowpass filters to prevent errors when the RF input signal-to-noise ratio is below a preset threshold.

In order to meet the interface requirements established by Auburn University, the input signal to the A/D converter must have a linear characteristic between zero and -1.8 volts for an $\underline{\ell}$ information phase measurement between $-\frac{\pi}{2}$ and $+\frac{\pi}{2}$ rads, and alternately, the same voltage range for an $\underline{m}$ information phase measurement between $-\frac{\pi}{2}$ and $+\frac{\pi}{2}$ rads. This arrangement allows the use of a single phase meter for both $\underline{\ell}$ and $\underline{m}$ information measurements. In order that the phase meter operate with no discontinuity over the range $-\frac{\pi}{4}$ to $+\frac{\pi}{4}$ rads, a delay line consisting of a $\frac{\pi}{4}\lambda$ segment of coaxial transmission line is inserted in the Direction Information Channel prior to the Positive Zero Crossing Detector. The insertion of this delay line eliminates errors (near phase measurements of zero degrees) due to zero crossing detector uncertainty. The output voltage requirement is met by proper adjustment of the dc gain at the output of $\underline{\ell}$ and $\underline{m}$ lowpass filters.

When there is insufficient signal strength in either Z or XY channels, the output of the bi-stable multivibrator is disconnected from the lowpass filter inputs by means of an inhibit gate. This gate is controlled by gating signal J, the development of which is covered in Sec. 5. The "memory" characteristic of the lowpass filters causes the S-band antennas to remain at the last direction stored in the filters. (This information is presumably the most recent and reliable information.)

* The development of switching signal L is covered in Sec. 6.

4.2 Phase Meter With Digital Output

A phase measurement circuit which overcomes some of the dc stability problems characteristic of the analog output phase meter described in the preceding section is shown in Fig. 4.2. The input signals are coupled to two positive zero crossing detectors as in the preceding section. These detectors produce start and stop pulses to a bi-stable multivibrator which generates a gating signal whose ON time t_ψ is proportional to the desired phase measurement ψ. This gating signal is applied through an OR gate to a count inhibit gate which switches a stable reference signal on and off to a digital counter. The stable reference signal is derived through frequency division of e_r, the 9.6 MHz reference signal coupled from the Station Control Receiver. Assuming integration over a time period equal to an integral number of cycles of the phase meter input frequency, the number of reference frequency cycles totaled in the digital counter is directly proportional to the measured phase ψ.

Gating signal K, coupled to the OR gate along with the output of the bi-stable multivibrator, is the signal controlling the integration time of the phase measurement; its derivation is covered in Sec. 6.2.

The counter must be read out at the end of the period of integration. This function is accomplished by a counter readout pulse, signal R, which causes the counter total at the end of the phase measurement integration period to be transferred to the digital converter through the readout gate. Signal R is developed in such a manner that counter readout will not occur if certain preestablished phase meter input signal criteria have not been met. Details of the development of this signal will be covered in Sec. 6.2.

The function of the digital converter is to convert the digital output of the counter into the 8-bit parallel form required for the input to the Auburn University Combinational Switching Network.[1] It will be noted that binary lines A

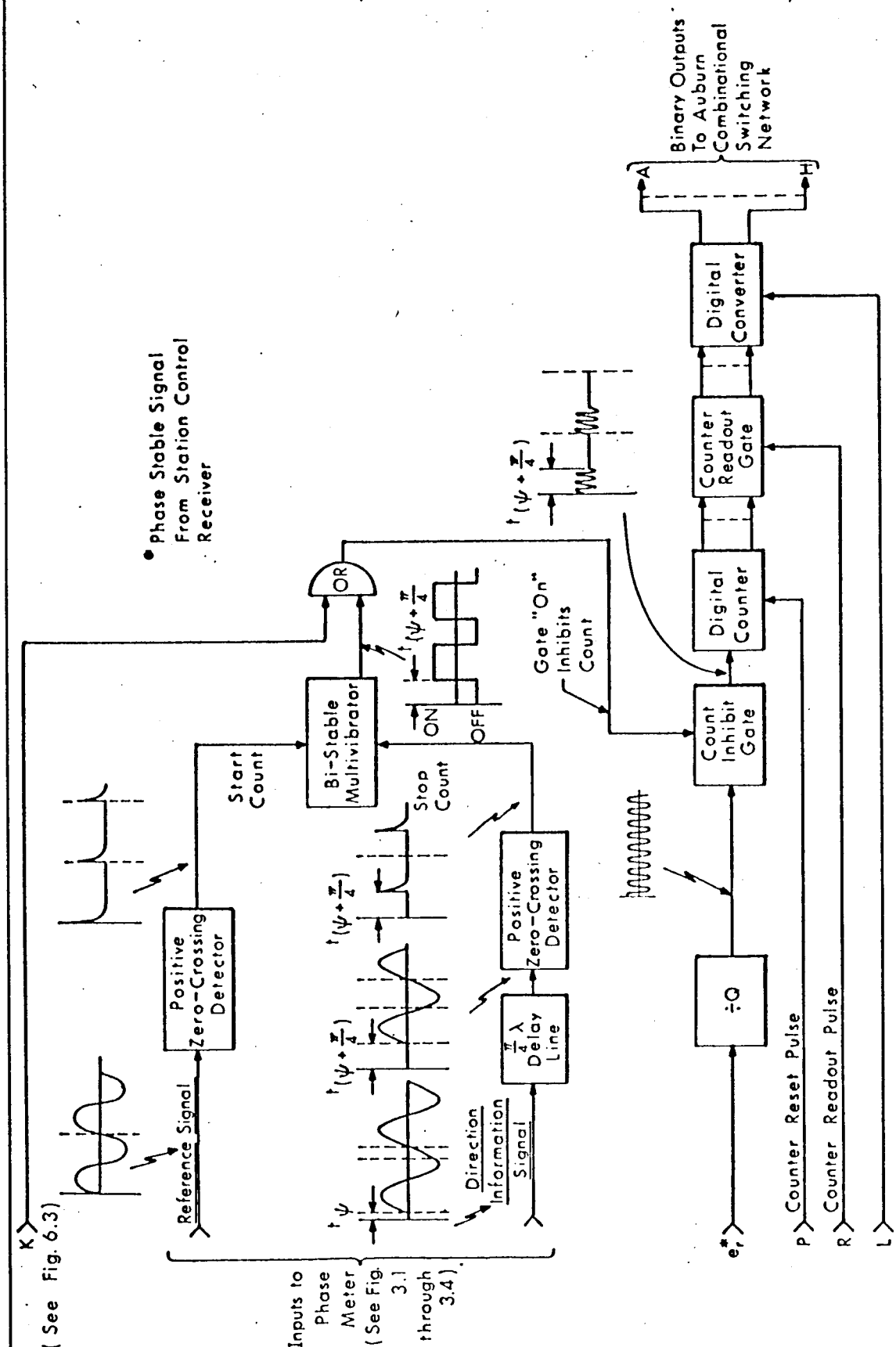

Fig. 4.2 Phase Meter With Digital Output.

through D contain the digitized value of ℓ, and lines E through H the digitized value of m*. Signal L is used to control the digital converter logic in such a way that at the end of the ℓ measurement period the output of the digital counter will be routed to output lines A through D. Similarly, signal L controls the digital converter logic so that at the end of the m measurement period the output of the digital counter will be routed to output lines E through H. Digital converter logic memory is such that if no readout pulse occurs at the end of the integration period, the S-band antennas will remain pointed at the direction wherein a readout pulse last occurred.

4.3 Phase Meter Zero Crossing Detector Requirements

The immunity to noise of both of the phase metering circuits described in this section is dependent to a large extent on the zero crossing detector circuitry employed. The design goal of any zero crossing detector is, of course, that it produce an output pulse at precisely the instant its input signal makes an amplitude transition across exactly zero voltage -- and only then. In all practical circuits, however, there is an input voltage range (which, for purposes of this discussion shall be called an "amplitude uncertainty range") over which a variance as a function of time exists as to the precise amplitude at which an output trigger pulse is produced. It is this characteristic which makes the zero crossing detector susceptible to output errors due to noise at low signal-to-noise ratios (SNR's). This error susceptibility is due to the fact that any minute input signal amplitude variations (e.g., noise) within the aforementioned "amplitude uncertainty range" may cause a false output trigger to be produced, and a resulting phase measurement error.

It is readily seen then, that for the application intended, the "amplitude uncertainty range" of zero crossing detectors must be extremely small in order

* Digit weighting is 8-4-2-1 for both ℓ and m.

to minimize phase measurement error at low SNR's. Most commercially available phase meters are not designed for operation in a high noise environment, and are thus prone to measurement errors at low SNR's. In addition, since they are primarily laboratory instruments, they are not stable over long periods of time, widely varying ambient temperatures, and large input signal dynamics. Thus, frequent adjustment is necessary when these laboratory instruments are required to operate in field conditions involving such variables as widely fluctuating ambient temperature.

Not mentioned in the above discussion of zero crossing detectors, but also important, is the time uncertainty of the output trigger pulse at high SNR's resulting from the zero crossing detector "amplitude uncertainty range." The measurement accuracy requirements of the D/B system proposed by Auburn University are of the order of a few tenths of a degree at the phase meter input carrier frequency. The corresponding zero crossing detector output trigger time certainty requirement is not a severe circuit design problem, and is satisfied by most zero crossing detectors at high input SNR's.

It is seen from the foregoing discussion that there is little likelihood of satisfying the D/F system phase meter requirements with commercially available laboratory phase meters. Therefore, in the design of a phase meter suitable for the D/F system proposed, particular attention should be given to the following:

a. Phase meter output accuracy should be commensurate with the measurement error budget.

b. The phase meter should be specifically designed to operate accurately and reliably at low input SNR's as well as when the input SNR is high.

c. The phase meter should be designed to function accurately and reliably over a wide ambient temperature range for long periods of time without adjustment.

d. The phase meter should be designed to operate over a wide dynamic range if large signal dynamics are expected at its input terminals.

5. RING SELECTION AND SWITCHING SIGNALS

The selection of either Z ring (vertically polarized elements) or XY ring (horizontally polarized elements) signals for S-band antenna steering is considered in this section, the criterion for this selection being which ring results in the more accurate S-band antenna steering information. Signal-to-noise ratios of RF signals in the system are convenient indicators of this accuracy. The two methods presented in this section depend on the measurement of this parameter. Each of the methods assumes that the reference channel represents the approximate SNR of its corresponding direction information channel.

5.1 AGC Voltage Comparison

In the first of the two methods, the selection of Z or XY rings is based simply on the amplitude comparison of AGC voltages from Z and XY reference channels. Noise power in the two reference channels is assumed equal. AGC voltages E and F (see Figs. 3.1 through 3.4) are coupled to a signal amplitude comparator, as shown in Fig. 5.1. The amplitude comparator is basically a differential

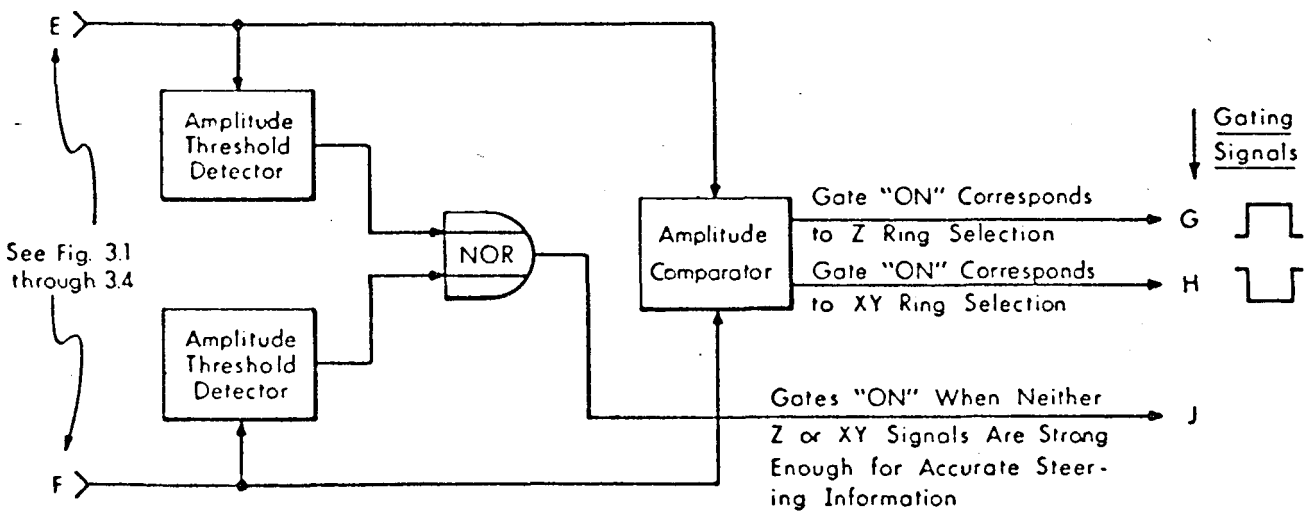

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Fig. 5.1 Derivation of Ring Selection Gating Signals from AGC Voltages

amplifier with only two stable states. If voltage E is greater than voltage F, the amplitude comparator gates the G signal ON; signal G is gated OFF if voltage F is greater than voltage E. Signal H, the complement signal of G, is also generated in the amplitude comparator. Gating signals G and H activate switches S_7 and S_8, respectively, thus switching either AGC voltage E or AGC voltage F to the reference channel AGC input. (see Figs. 2.1 & 2.2)

AGC signals E and F are also coupled to amplitude threshold detectors, which gate ON when the AGC voltage reaches a predetermined threshold level. The gating signals from the amplitude threshold detectors are coupled to a NOR circuit, which gates ON only when neither Z or XY signals is strong enough for accurate S-band antenna steering, as determined by the preset thresholds. The NOR logic circuit output is called signal J, an inhibit gate used to cause the S-band antenna to remain at the last direction wherein reliable pointing information was received.

5.2 Alternate Ring Selection Method

An alternate method of selecting the ring most likely to provide the most reliable S-band antenna steering information is the one suggested in Fig. 5.2, which replaces the circuit of Fig. 3.3. This method can only be employed when conventional IF filtering is used, such as with the three-channel receiver of Fig. 2.1.*

Utilizing this technique, output signals from Z and XY channels in the D/F receiver, e_3 and e_4**, respectively, are coupled to bandpass

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* This limitation is based on the narrow filter bandwidths required in the circuit (e.g., B_{nar}) and the Q ranges available in conventional filters. The low IF center frequencies thus required are characteristically available in a triple conversion receiver such as that of Ref. 4. Implementation of this technique when PLL's are used as filter elements is not desirable.

** See Fig. 2.1 for derivation of e_3 and e_4.

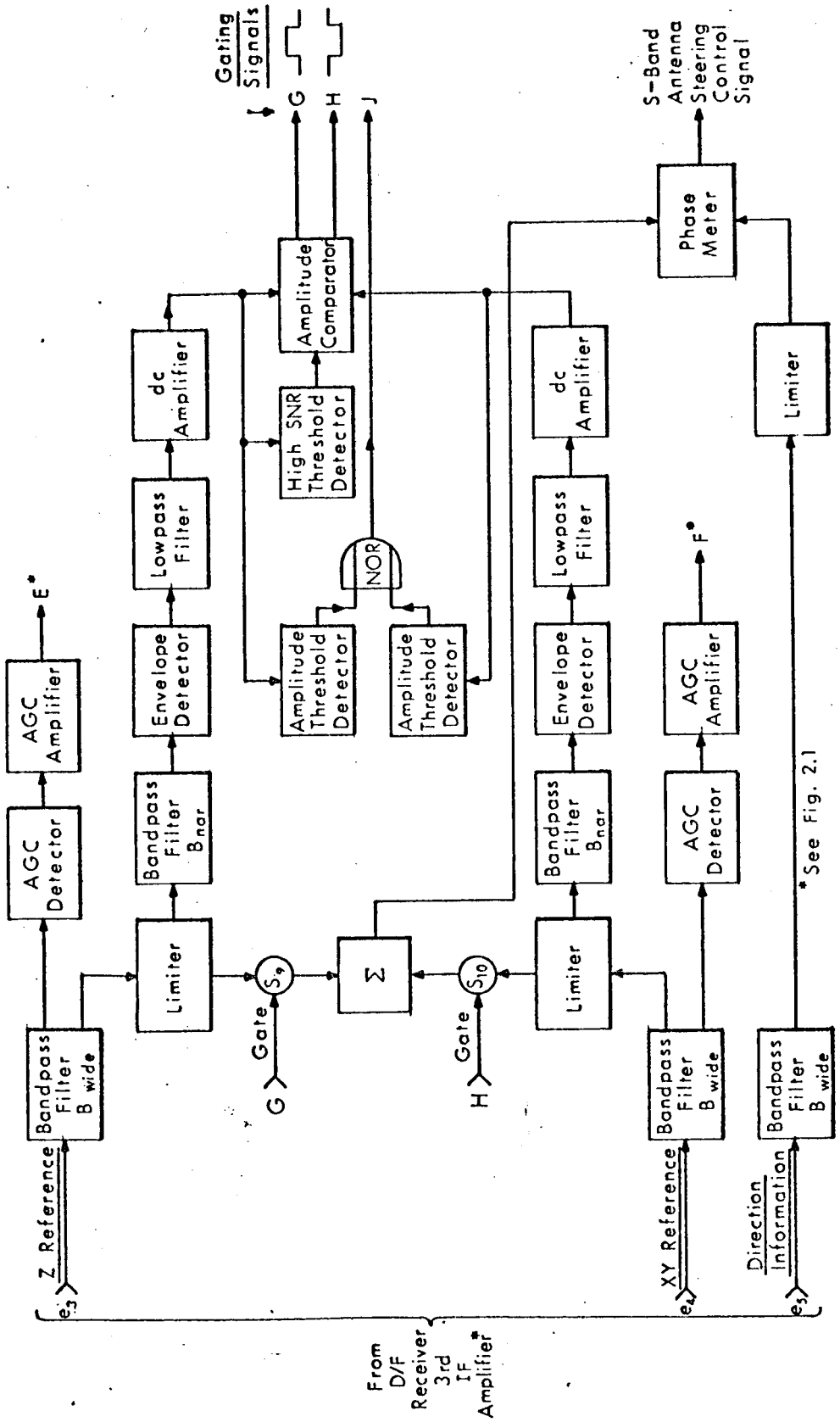

Fig. 5.2 Alternate Method for Derivation of Ring Selection Gating Signals.

filters with noise bandwidths B_{wide}. The bandpass filter output signals are then coupled to limiters, where they are amplitude limited. The power spectrum $P_t(f)$ out of the first bandpass filter is given by:

$$P_t(f) = S(f) + N(f) \tag{5.1}$$

where:

P_t = total power at the output of the first bandpass filter,

S = signal power at the output of the first bandpass filter, and

N = noise power at the output of the first bandpass filter.

The power spectrum of Eq.(5.1) is shown in Fig. 5.3.

The output power spectrum of the first limiters in Fig. 5.2 is given by:

$$P_\ell(f) = S_\ell(f) + N_\ell(f) \tag{5.2}$$

where:

P_ℓ = total power at the output of the first limiter,

S_ℓ = signal power at the output of the first limiter, and

N_ℓ = noise power at the output of the first limiter.

The power spectrum of Eq. (5.2) is depicted in Fig. 5.4a. Corresponding signal and noise powers as functions of signal-to-noise ratio are shown in Fig. 5.4b.

Signals in the two channels are coupled from the first limiter to a second bandpass filter with noise bandwidth B_{nar}, as shown in Fig.5.2. The output spectrum of the two signals is then:

$$P_o(f) = S_\ell(f) + N_o(f) \tag{5.3}$$

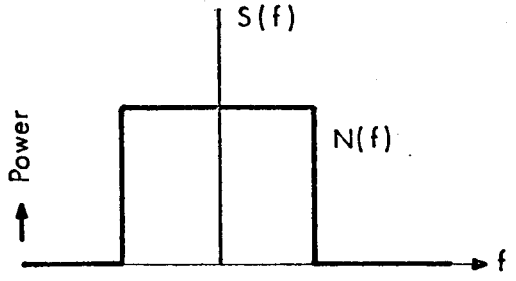

Fig. 5.3. Power Spectrum of Signal and Noise at Input to First Limiter

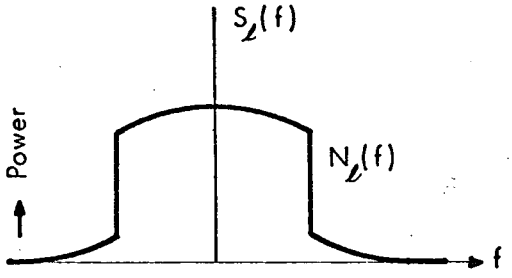

Fig. 5.4a. Power Spectrum of Signal and Noise at Output of First Limiter

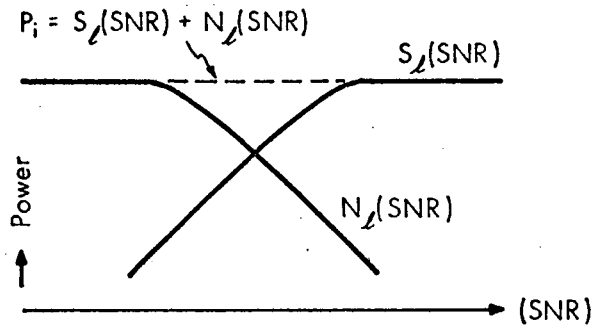

Fig. 5.4b. Signal and Noise Power at First Limiter Output as a Function of SNR

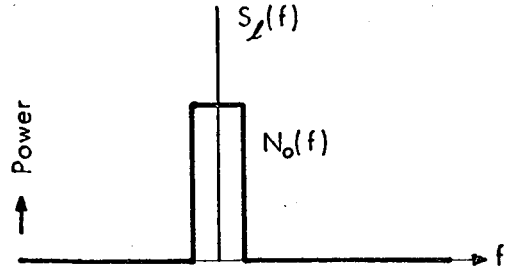

Fig. 5.5a. Power Spectrum of Signal and Noise at Output of Narrow Bandpass Filter

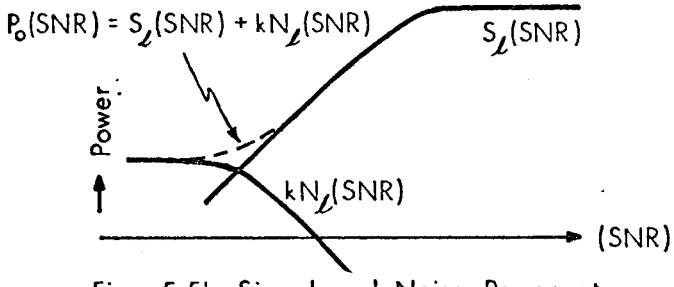

Fig. 5.5b Signal and Noise Power at Narrow Bandpass Filter Output as a Function of SNR

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where:

P_o = total power at the output of the second bandpass filter, and

N_o = noise power at the output of the second bandpass filter.

The power spectrum of Eq.(5.3)is shown in Fig. 5. 5a.

N_o in Eq. (5. 3)is equal to kN_ℓ where

$$k = \frac{B_{nar}}{B_{wide}} \tag{5.4}$$

Therefore:

$$P_o\,(SNR) = S_\ell\,(SNR) + k\,N_\ell\,(SNR) \tag{5.5}$$

Equation (5. 5) is graphically represented by Fig. 5. 5b.

Following the second bandpass filter, the signals are coupled to envelope detectors and lowpass filters. The dc signals from the post-detection filters are then coupled to an amplitude comparator, where gating signals G and H are developed in a manner similar to that shown in Fig. 5. 1. As in Fig. 5. 1, gating signal G "ON", corresponds to Z ring selection and gating signal H "ON" corresponds to XY ring selection.

Total power to the envelope detectors as a function of SNR is re-drawn in more detail in Fig. 5. 6. Note that if both Z and XY ring SNR's at the inputs to the first limiters are higher than approximately + 10 dB, the amplitude comparator will not distinguish accurately between the amplitudes of the two dc signals representing SNR. A high SNR detector is therefore employed as shown in Fig. 5. 2 which provides a gate output if the Z ring SNR exceeds a preset threshold (e. g., + 10 dB input SNR). This detector causes G and H signals to gate in such a manner that Z ring signals are always selected in preference to that of the XY ring (when both Z and XY ring SNR's

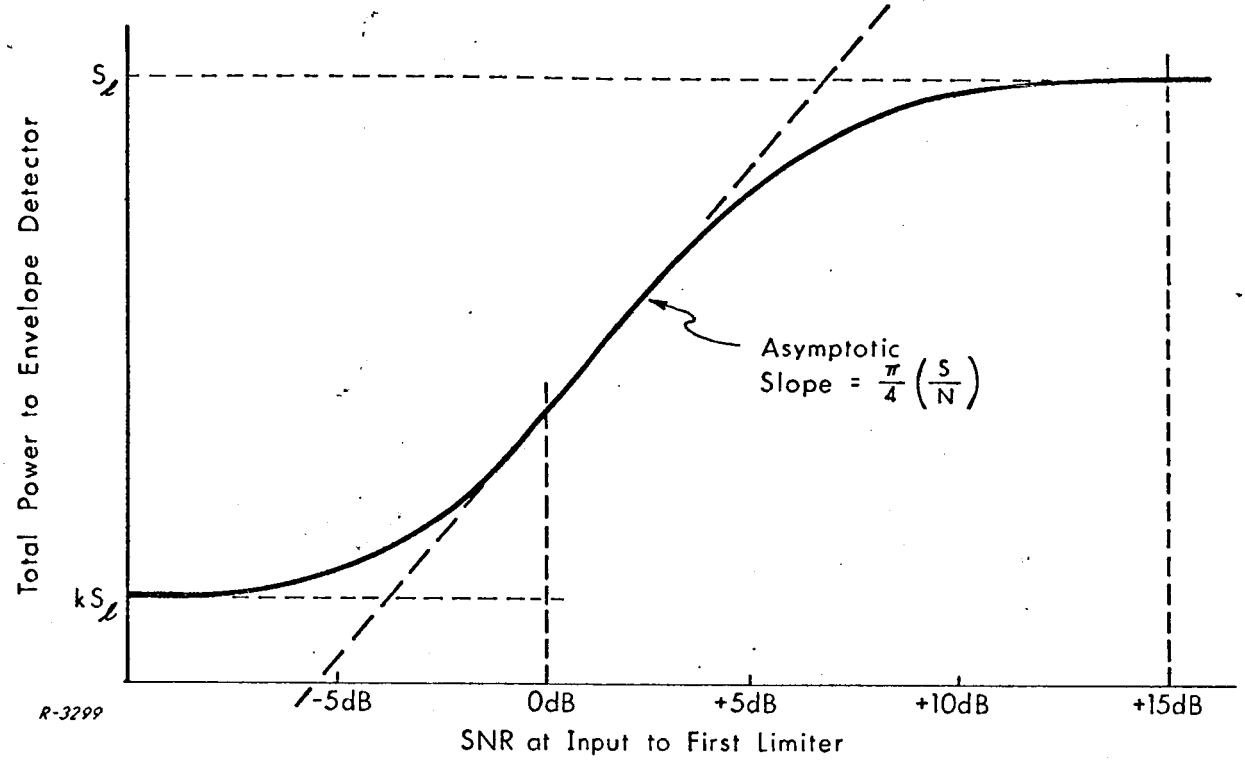

Fig. 5.6 Input/Output Characteristics of Alternate Method Ring Selector SNR Detector.

are high) because sea (or earth) reflected multipath signals are of lesser amplitude in vertically polarized received waves than in those horizontally polarized. Consequently, less interference (in the form of phase and amplitude distortion) is likely to be present on the received signal, and thus greater S-band antenna steering accuracy is achieved. Selection of Z ring signals when both channels have high SNR's could similarly be incorporated in the subsystem design of Fig. 5.1, if desired.

The choice of k (see Eq. 5.4) becomes one of selection of B_{nar}, since the noise bandwidth requirement B_n of the D/F receiver dictates B_{wide}.* B_{nar} should be chosen so that the maximum slope of the curve of Fig. 5.6 occurs in the input SNR region 0 dB < SNR_{in} < +15 dB, since the phase meter threshold is in this range.[3]

* The bandpass filters in Fig. 5.2 with bandwidths B_{wide} are the same filters as those in Fig. 3.3 with bandwidth B_n.

AGC voltages E and F and gating signal J are developed in an identical manner to that depicted in Fig.5.1. Inputs to S_9 and S_{10} are the outputs of limiters from Z Reference and XY Reference channels, respectively, instead of directly from bandpass filters B_{wide} (or B_n, in the circuits of Fig.3.3). Limiting is also shown in the Direction Information channel prior to the phase meter input, so that both signal inputs to the phase meter will be of equal amplitude under varying conditions of D/F system input signal dynamics. The necessity for limiting prior to the phase meter inputs is dependent on the type of phase meter employed (see Sec. 4.), and indeed may not be necessary or even desirable with certain D/F receiver configurations.

6. TIMING AND CONTROL SIGNALS

In the various D/F receiver designs presented in Sec. 2, $\underline{\ell}$ and $\underline{m}$ information have been shown to be derived sequentially, since the direction information changes very slowly and this arrangement requires the least equipment. A one-half second sampling period for $\underline{\ell}$ information, followed by an equal period for $\underline{m}$ information (making the total sample set period one second), has been suggested. Such a period appears consistent with steering accuracy requirements and the need for information updating based on expected antenna pointing direction angular change rates.

The need exists, then, for clocked gating signals which cause $\underline{\ell}$ and $\underline{m}$ signal outputs to be switched alternately to the single Direction Information channel in the D/F receiver. In order that the S-band antennas be directed toward the space vehicle in the shortest time after initial reception of the VHF station control signal, the $\underline{\ell}$ and $\underline{m}$ sample set period should begin at precisely the moment of D/F receiver signal acquisition.

In addition to $\underline{\ell}$ and $\underline{m}$ sequencing gates, various other gating and pulse signals are required for phase metering circuitry.

It is the purpose of this section to show how each of these signals is developed.

6.1 Clock Gating Signals

The development of basic clock gating signals for alternate switching of $\underline{\ell}$ and $\underline{m}$ information to the D/F receiver is shown in Fig. 6.1. This circuit is applicable to receivers employing either an analog- or digital-type phase meter.

The 1.2 MHz reference signal from the Station Control Receiver is frequency divided to a digital counter input frequency commensurate with the number of counter stages and the readout resolution required. The function of

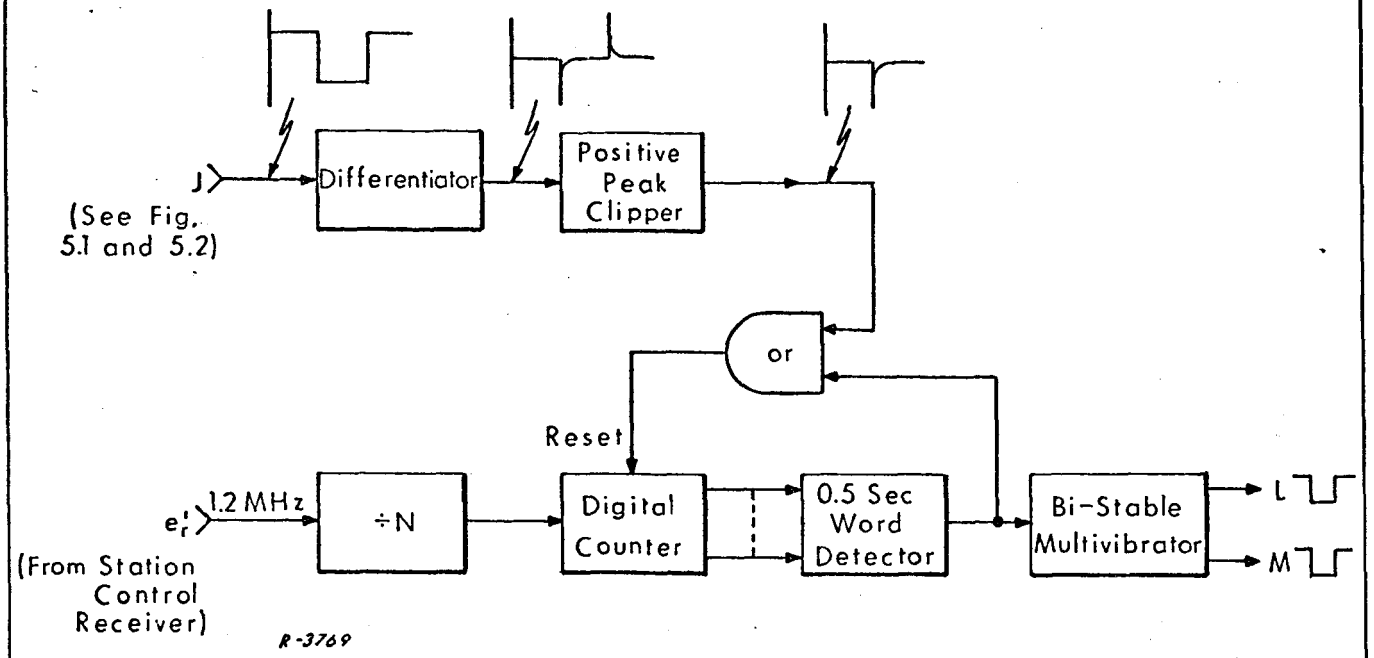

Fig. 6.1 Basic Clock Gating Signal Generator

the digital counter is to accumulate a count of the total number of cycles of the frequency divided reference, beginning with the counter reset. At the end of approximately 0.5 second the 0.5 second word detector, an AND gate, triggers a bi-stable multivibrator to its opposite stable state. Complement gating signals L and M are developed in this multivibrator stage. These signals are used ultimately to switch the RF signals developed in the front end of the D/F receiver,* and in case an analog-type phase meter is employed, its phase meter lowpass filter inputs and outputs are also switched by signal L (see Sec. 4.1).

The output of the 0.5 second word detector is coupled through an OR gate to reset the digital counter at the end of each 0.5 second. A change of state of L and M gating signals thus occurs in time coincidence with these reset pulses.

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* See Secs. 2.2, 2.3, and 6.3.

In order to steer the AROD System S-band antennas to the proper direction in the minimum possible time after initial acquisition* of the VHF signal, it is necessary that the measurement period of an $\underline{\ell}$ and $\underline{m}$ information set begin at precisely the moment of VHF signal acquisition. This moment is indicated in time by the negative-going transition of signal J.** Thus, to obtain a pulse which corresponds in time to initial acquisition of the VHF signal, signal J is differentiated and passed through a positive peak clipper. The resultant signal is coupled through the OR gate referred to above to reset the digital counter, and an $\underline{\ell}$ and $\underline{m}$ measurement period is initiated.

It will be observed that the digital counter can be reset by either an output from the 0.5 second word detector (in which case an $\underline{\ell}$ and $\underline{m}$, or $\underline{m}$ and $\underline{\ell}$, measurement period is initiated) or a negative-going transition of signal J. Were signal J to make more than one negative-going transition per 0.5 second interval for a period of several seconds;*** however, it can be seen that the counter would not be reset during this period and only one information set component (either all $\underline{\ell}$ or all $\underline{m}$ information) would be measured. It is therefore necessary to provide for this occurrence in the design of the clock gating signal generator.

Figure 6.2 shows an improved version of the circuit of Fig. 6.1. The negative pulse from the positive peak clipper is inhibited from resetting the 0.5 second digital counter by the reset gate if the reset gate bi-stable

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* For definition of the term "acquisition," as used here, refer to the footnote in Appendix B, page

** See Sec. 5 for the development of signal J.

*** This condition would be encountered, for instance, if the received signal level at the inputs to the J signal amplitude threshold d detectors varied about the threshold levels. Such a condition could be caused by such phenomena as signal propagation characteristics, vehicle tumbling, multipath, etc.

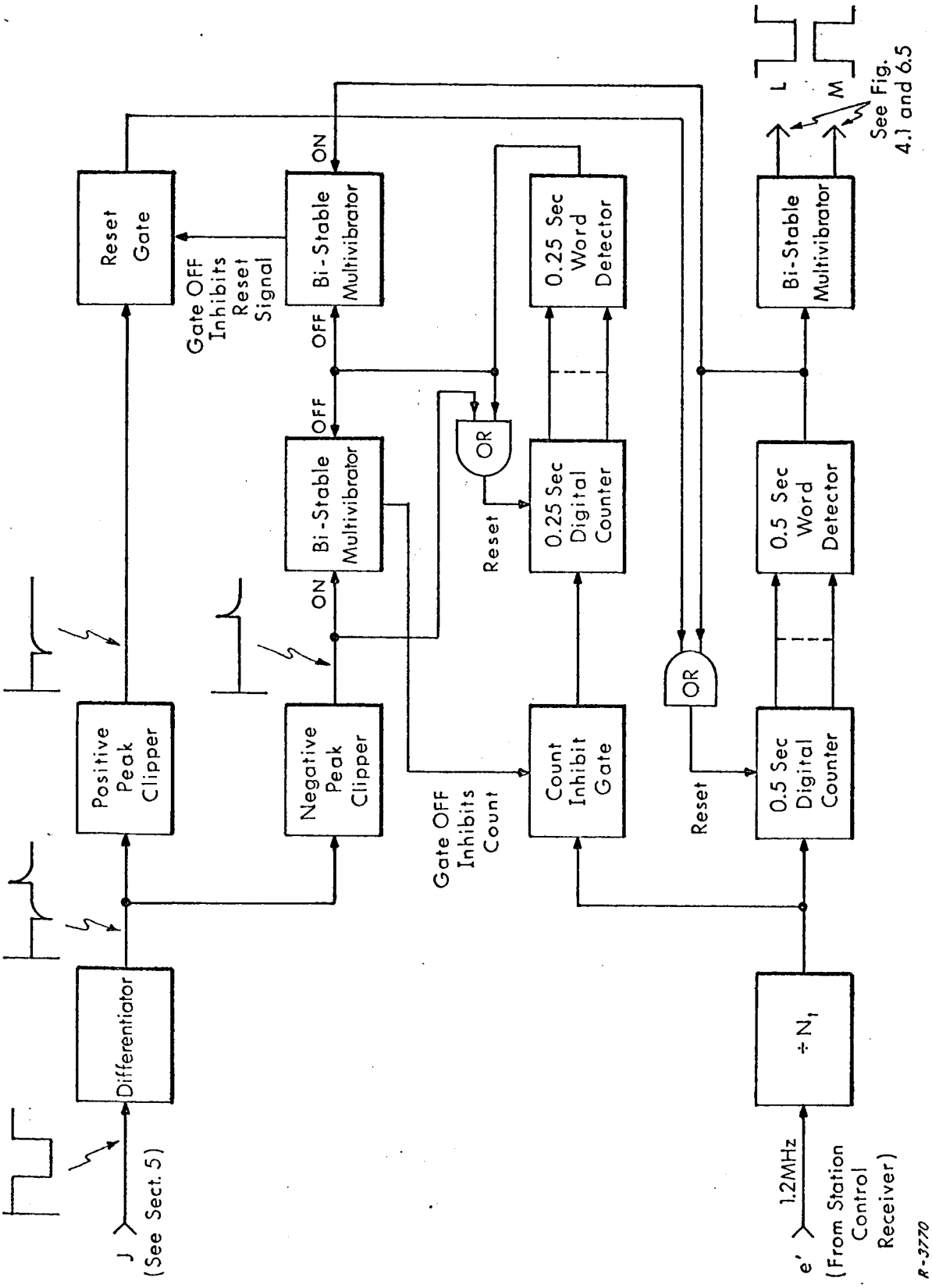


Fig. 6.2 Improved Clock Gating Signal Generator

multivibrator is in an ON state. Thus, when the inhibit signal to the reset gate in ON, the 0.5 second counter is allowed to accumulate a count of the frequency divided reference until the 0.5 second word detector detects coincidence and (1) changes the state of the L and M signal multivibrator, (2) resets the 0.5 second digital counter, and (3) switches the reset bi-stable multivibrator ON to allow the presence of a reset pulse from the positive peak clipper to reset the 0.5 second digital counter.

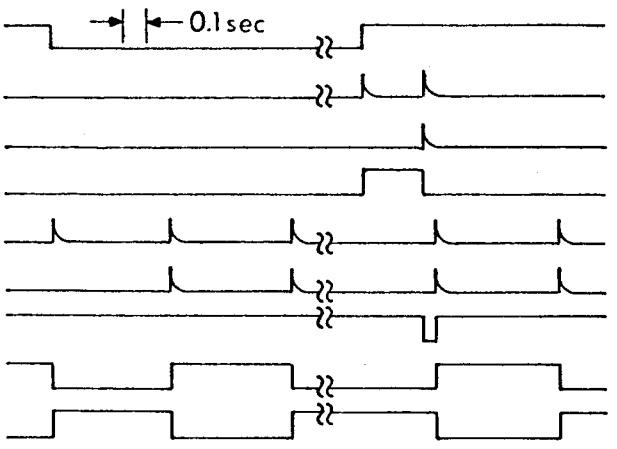
The 0.25 second counter and word detector act as a timing circuit to allow the positive peak clipper reset signal to reset the 0.5 second digital counter only after cessation of signal occurs for a period of 0.25 second or more. By utilizing this additional circuitry, rapid transitions of state of signal J do not cause the 0.5 second counter to reset before the 0.5 second word detector is allowed to trigger the L and M signal bi-stable multivibrator to its opposite stable state. The condition is thus established that 0.25 second period must elapse after a signal has been initially acquired before a second negative-going pulse from the positive peak clipper is allowed to reset the 0.5 second digital counter.

The net effect of the circuit of Fig. 6.2 is that it causes the transition from $\underline{\ell}$ to $\underline{m}$ information, or vice versa, to occur at least every 0.75 second, but not more frequently than every 0.5 second. The circuit also causes an $\underline{\ell}$ and $\underline{m}$ phase measurement period to begin exactly at the time of initial RF signal interception, as determined by signal J. Near the signal acquisition threshold, when signal J transitions from OFF to ON at frequent, random intervals, the circuit logic causes a decision to be made that the RF signal is an initially intercepted signal (and thus causes an $\underline{\ell}$ to $\underline{m}$ or $\underline{m}$ to $\underline{\ell}$ transition) only if the RF signal has not been present for at least 0.25 seconds following the last free-running $\underline{\ell}$ to $\underline{m}$ or $\underline{m}$ to $\underline{\ell}$ signal logic transition.

Figure 6.3 shows the timing relationship between logic stages in Fig. 6.2 for three typical RF input signal cases.

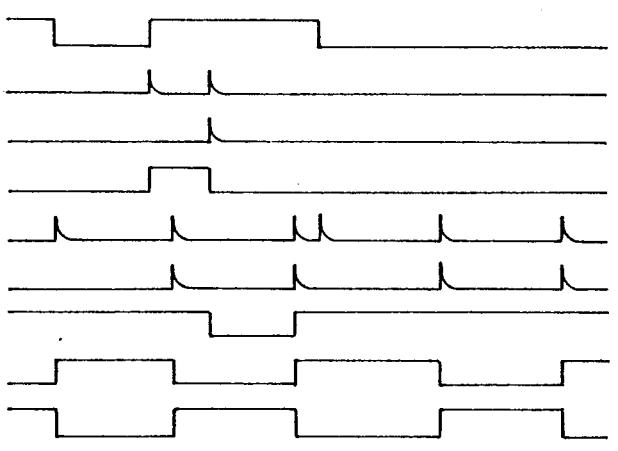
CASE 1:

Signal J	No Sig Signal
0.25 sec Counter Reset	Reset Off
0.25 sec Word Detector	Word Off
0.25 sec Word Counter	Accum Inhibit
0.5 sec Counter Reset	Reset Off
0.5 sec Word Detector	Word Off
Reset Gate	On Off
L Signal	1 0
M Signal	1 0



CASE 2:

Signal J	No Sig Signal
0.25 sec Counter Reset	Reset Off
0.25 sec Word Detector	Word Off
0.25 sec Word Counter	Accum Inhibit
0.5 sec Counter Reset	Reset Off
0.5 sec Word Detector	Word Off
Reset Gate	On Off
L Signal	1 0
M Signal	1 0



CASE 3:

Signal J	No Sig Signal
0.25 sec Counter Reset	Reset Off
0.25 sec Word Detector	Word Off
0.25 sec Word Counter	Accum Inhibit
0.5 sec Counter Reset	Reset Off
0.5 sec Word Detector	Word Off
Reset Gate	On Off
L Signal	1 0
M Signal	1 0

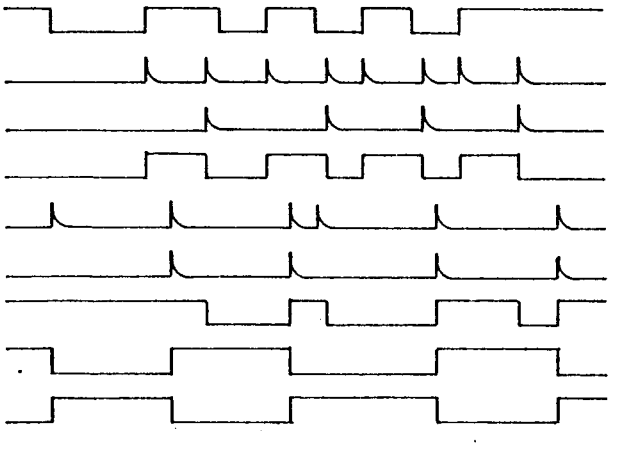


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Fig. 6.3 Timing Relationships in Circuit of Fig. 6.2

6.2 Functional Control Signals for Digital Phase Meter

As has been stated, the generation of basic clock gating signals for alternate switching of ℓ and m information to the D/F receiver wherein a digital-type phase meter is employed is basically the same as shown in Fig. 6.2. Additional control signals are required, however, for the digital phase meter. The method for development of these additional signals - namely signal K, R, and P - is shown in Fig. 6.4.

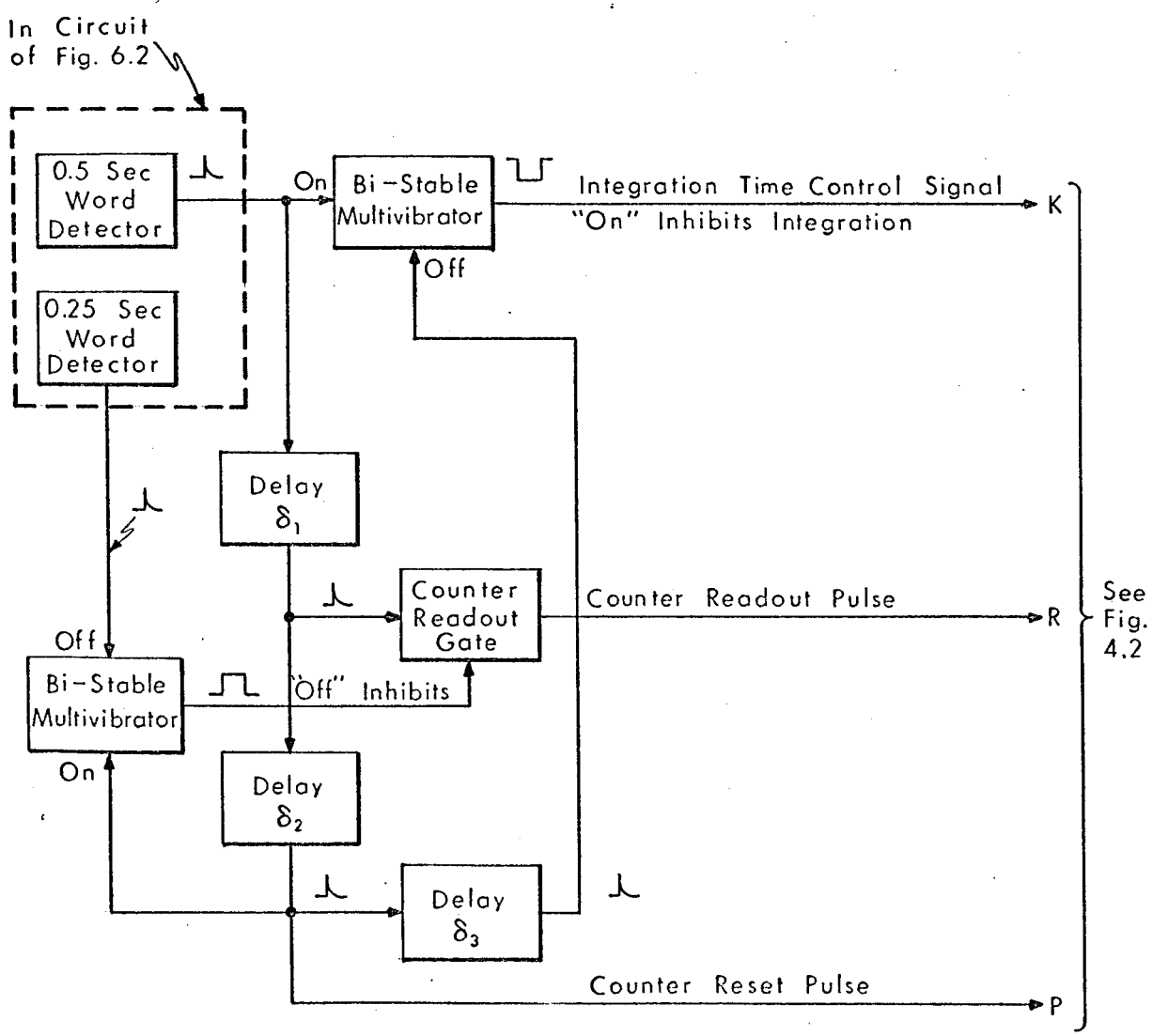

Fig. 6.4 Generation of Control Signals for Digital Phase Meter

The operation of this circuit is as follows: A pulse from the 0.5 sec word detector in Fig. 6.2 occurs when there is a change of state from $\underline{\ell}$ to $\underline{m}$ or from $\underline{m}$ to $\underline{\ell}$ information. This pulse triggers a bi-stable multivibrator to its ON state, thus inhibiting phase measurement integration through control signal K (see Sec. 4.2). If the counter readout gate is ON, the output pulse from the 0.5 sec word detector is coupled through time delay circuitry with delay δ_1, and becomes signal R. The phase measurement digital counter is caused to be read out by signal R (see Fig. 4.2).

Signal R is further delayed through time delay δ_2, and following this delay becomes signal P, the counter reset signal. Following counter reset with signal P, the pulse is again delayed, this time through delay δ_3, and is used to reset the integration time delay multivibrator to its OFF state. The integration time control signal, signal K, is thus generated as an output of the bi-stable multivibrator. The total integration inhibit time (or signal K OFF time) is $\delta_1 + \delta_2 + \delta_3$, which can presumably be made to be an integral number of cycles of the reference signal carrier frequency, and is taken into account in the integration time averaging proportionality factor.

If a signal dropout occurs longer than 0.25 second, there will be a pulse output from the 0.25 sec word detector (see Fig. 6.2). This pulse triggers the counter readout bi-stable multivibrator in Fig. 6.4 to its OFF state, and the counter readout gate inhibits signal R, the counter readout pulse. Thus, the digital counter used to make the $\underline{\ell}$ and $\underline{m}$ phase information measurements is not read out if a signal dropout lasting more than 0.25 second occurs during any $\underline{\ell}$ or $\underline{m}$ measurement period. The counter readout bi-stable multivibrator is reset by the counter reset pulse (signal P) at the end of the $\underline{\ell}$ or $\underline{m}$ measurement period to permit counter readout during the subsequent $\underline{\ell}$ or $\underline{m}$ information measurement period. When the counter is not caused to be read out by signal R, the digital converter logic memory in the phase meter (see Fig. 4.2) causes the last reliable phase measurement made to control the steering of the S-band antennas.

6.3 RF Routing Control Signals

The RF routing control signals required for the D/F receiver designs of Sec. 2 are generated as shown in Fig. 6.5. Signals A, B, C, and D are gated ON in accordance with the following logic table.

Signals	G	H	L	M
A	ON	OFF	ON	OFF
B	ON	OFF	OFF	ON
C	OFF	ON	ON	OFF
D	OFF	ON	OFF	ON

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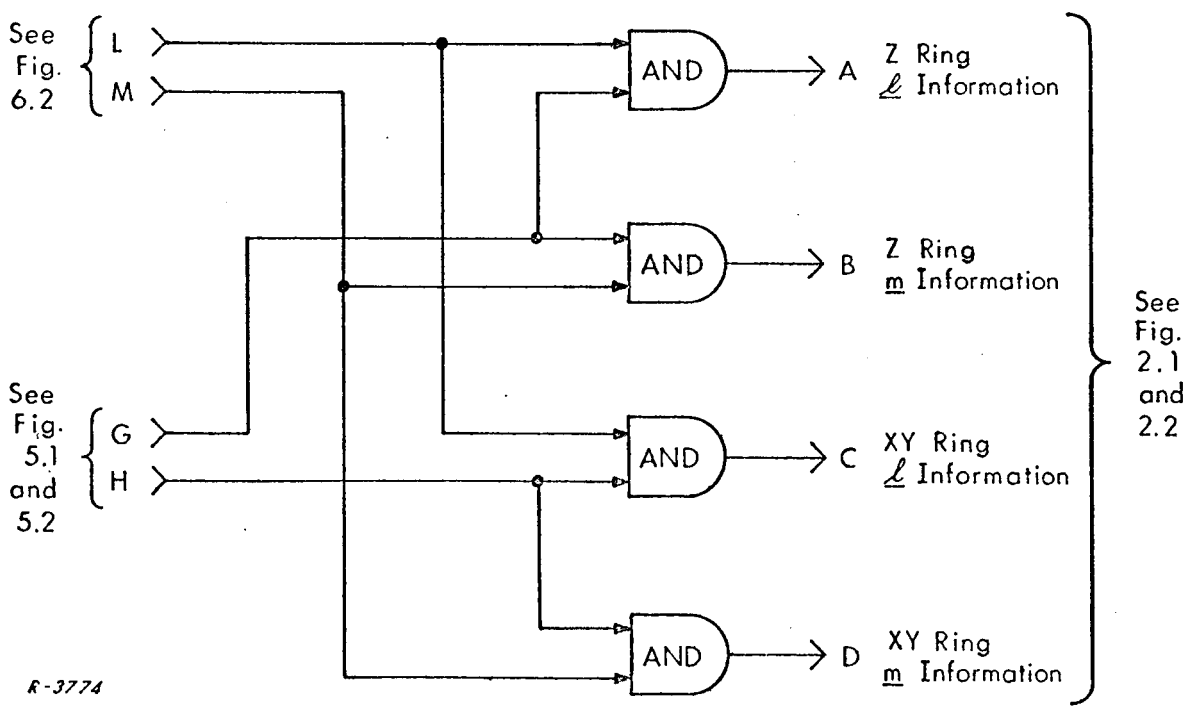

Fig. 6.5 Development of RF Routing Control Signals

7. CONCLUSIONS

It is clear that because of the threshold differences[4] between the Station Control Receiver and the Direction-Finding Receiver, the D/F receiver design proposed in Reference 1 is not adequate. Summarized, therefore, in this report are several alternate D/F receiver designs which will provide the required thresholds, as well as other features highly desirable due to the requirement for long-term stability and other unique requirements characteristic of the D/F system under development.

At the time of this writing, an AROD system D/F receiver had been designed and fabricated whose performance was reportedly superior to that design proposed in Reference 1. A detailed analysis of this new equipment has not been accomplished by ADCOM.

Recent technological advances suggest that the functions now requiring the existence of a VHF control link in the AROD system could now be absorbed practically into the two S-band links in the present system. ADCOM believes that this possibility is worthy of analytic investigation, and recommends such a project for future consideration.

8. REFERENCES

1. Final Report, "Automatically Scanned Antenna Systems," prepared for George C. Marshall Space Flight Center by Auburn University Antenna Research Laboratory under NASA Contract No. NAS 8-11251, E. R. Graf, Project Leader, pp. 31-32, January 20, 1966.

2. Technical Report No. 2, "Special Studies of AROD Systems Concepts, and Designs," prepared by ADCOM, Inc. for George C. Marshall Space Flight Center under Contract NAS 8-20128, October 15, 1965.

3. Ibid, Sec. 3.2.

4. Ibid, Sec. 3.1.

APPENDIX A

ANALYSIS OF DOPPLER FREQUENCY SHIFT ON LOCAL OSCILLATOR SIGNALS OF STATION CONTROL RECEIVER

The block diagram of the Station Control Receiver is shown in Fig. A.1. The doppler frequency components of voltages e_1 and e_2 are computed below as a function of doppler frequency shift on the station control signal.

Writing the loop frequency equations for the Station Control Receiver

$$f_c - 3f_2 - f_2 = 9.6 \text{ MHz} \tag{A.1}$$

$$f_2 = 0.25\, f_c - 2.4 \text{ MHz} \tag{A.2}$$

Since $f_1 = 3f_2$,

$$f_1 = 0.75\, f_c - 7.2 \text{ MHz} \tag{A.3}$$

From Eqs. (A.2) and (A.3) it can be seen that

$$\delta_2 = 0.25\, \delta_c \tag{A.4}$$

and

$$\delta_1 = 0.75\, \delta_c \tag{A.5}$$

where δ_c, δ_2 and δ_1 are doppler frequency shifts on f_c, f_2 and f_1 respectively. Under the conditions that $\delta_c = \pm .6$ kHz,

$$\delta_2 = \pm 1.5 \text{ kHz} \tag{A.6}$$

and

$$\delta_1 = \pm 4.5 \text{ kHz} \tag{A.7}$$

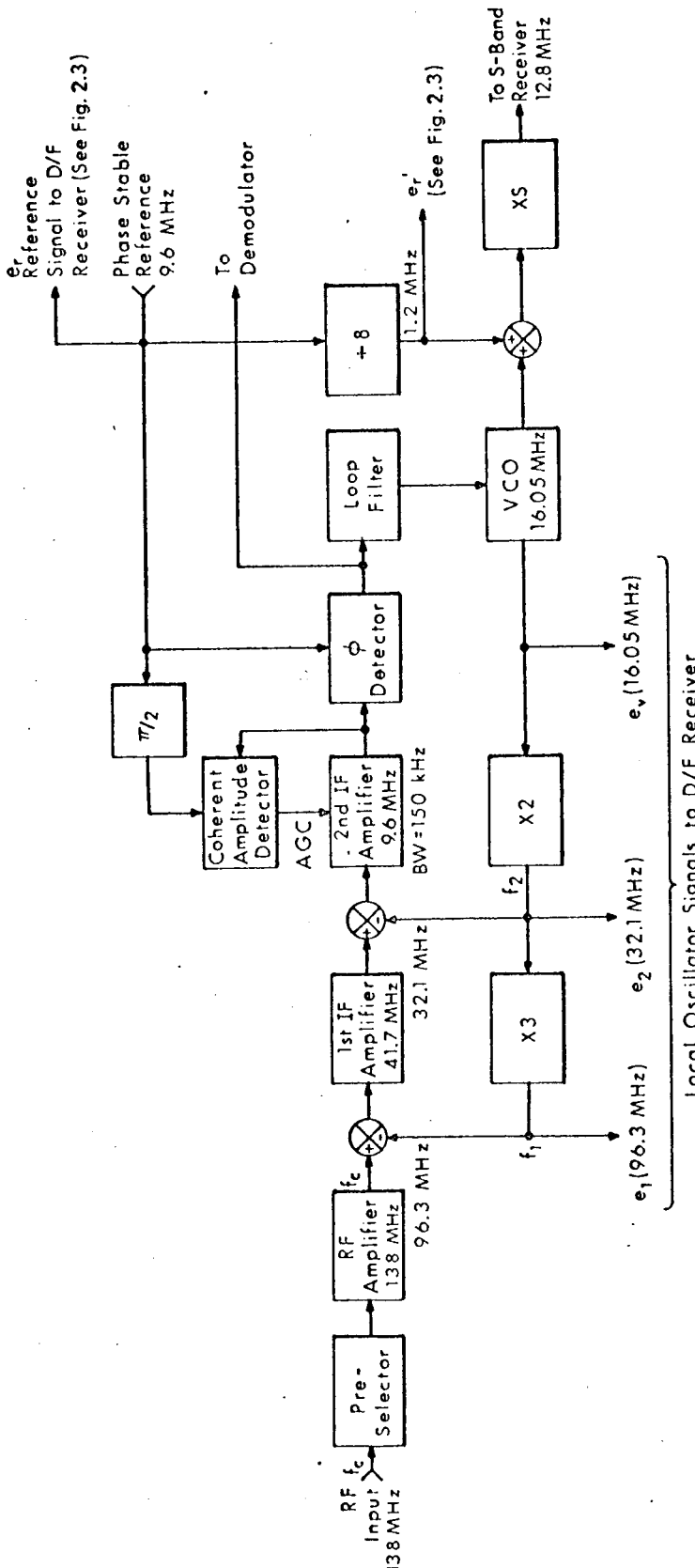

Fig. A.1 Station Control Receiver.

APPENDIX B

PHASE METER OUTPUT FILTERING

Lowpass filtering is required at the output of the phase meter to reduce the noise coupled to the A/D converter. Sequential sampling of $\underline{\ell}$ and $\underline{m}$ information results in a different dc level at the output of the phase meter during the period of $\underline{\ell}$ information sampling than for the period of $\underline{m}$. A single filter section such as that shown in Fig. B.1 could be employed to provide the necessary filtering, but since two output signals are alternately present, an error would exist until the capacitor in the filter charged to the analog value of the new signal.

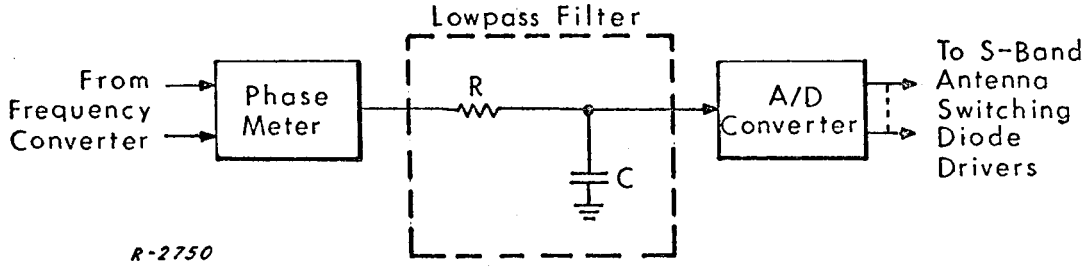

Fig. B.1 Phase Meter Output Coupled to Single Section Lowpass Filter.

The presence of such an error each time the input signal is switched would require a filter with a very short time constant in order that the total error be kept within acceptable limits.

A better approach for accomplishing the necessary filtering is the one shown in Fig. B. 2.

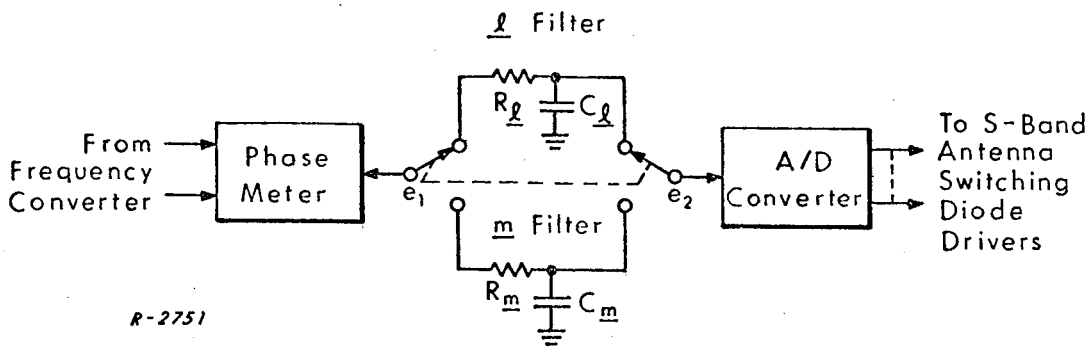

Fig. B. 2 Phase Meter Output Switched Between Two Lowpass Filters.

The inputs and outputs of two separate filters are switched synchronously with the sampling periods of ℓ and m information. During the period of ℓ information sampling, the ℓ filter capacitor charges to the dc level representing ℓ information. When the input signal is switched to m information, the m filter capacitor charges to the dc level representing m information. During the m filter charge period, the input and output of the ℓ filter are disconnected, and since there is no load on the ℓ capacitor, ℓ information is stored in the ℓ filter during the charge period of the m filter. Similar storage of m information occurs during the period of ℓ filter capacitor charge.

A switching period of one second for ℓ and m information sampling has been suggested. Such a period would result in ℓ and m filter integration times of 0. 5 second each, assuming alternate sampling. Information storage occurs during the half-period the alternate filter is integrating.

The upper bound of the filter time constant is determined by the amount of error to be tolerated due to filter capacitor charge lag. In the period immediately following signal acquisition this charge lag is potentially greatest. After the transient error caused by the acquisition process has subsided, only two sources of error remain: (1) error due to filter capacitor leakage, either internal or through the A/D converter load, and (2) error due to vehicle flight dynamics. The error due to capacitor leakage may be made negligible by proper selection of the type* and value of the filter capacitor. The error due to vehicle dynamics is a consideration solely of the filter time constant, assuming an ideal system. This time constant should be sufficiently short that when the rates of change of $c\ell$ and cm are maximum, the error is within tolerable limits. This condition will be satisfied if the time constant is chosen to result in an acceptable acquisition transient error with a maximum initial $c\ell$ or cm offset.

The filter time constant lower bound is determined by the error to be tolerated due to noise. The time constant chosen to satisfy the error requirement imposed by the filter capacitor charge lag will easily fulfill the lower bound time constant constraint.

B.1 Maximum Rates of Change of $c\ell$ and cm

The near-earth orbital path of the vehicle is shown in the diagram of Fig. B.3.

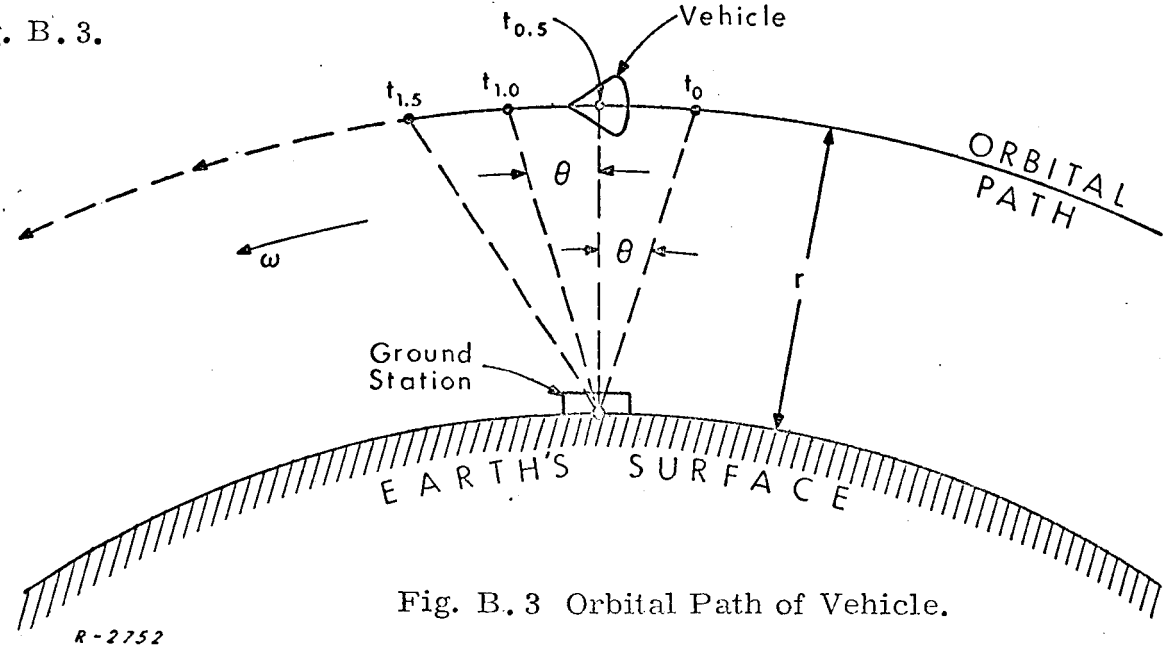

Fig. B.3 Orbital Path of Vehicle.

*i.e., one with low loss characteristics

From the AROD system specifications, the maximum vehicle velocity v_{max} that the system is required to handle is 12,000 meters per second. The minimum range r_{min} over which the system is required to operate is 100 km. Thus, the maximum rate of change ω_{max} of $c\ell$ or cm which could be expected is approximately:

$$\omega_{max} \approx \frac{v_{max}}{r_{min}} = 0.12 \text{ rad/sec}$$

$$= 6.87 \text{ degrees/sec} \qquad \text{(B. 1)}$$

B. 2 Transient Error Following Signal Acquisition

For computation of the transient error immediately following the acquisition* of a signal, the maximum possible offset of $c\ell$ or cm (with respect to the ambient charge on the filter capacitor) is assumed.

The charge on the filter capacitor due to a step input in voltage is given by the following equation:

$$e_2(t) = e_1\left(1 - e^{\frac{-t}{\tau}}\right) \qquad \text{(B. 2)}$$

where:

$e_2(t)$ = filter output, degrees**

e_1 = amplitude of filter input, degrees**

t = time, seconds

τ = RC = filter time constant, seconds

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*The term "acquisition," as used here, is defined to mean the first instant of reception of a signal wherein the input level is such that extraction of useful information by the phase meter is possible.

**For convenience in notation, input and output voltages of the post-detection filter will be expressed directly in "degrees," since these potentials are analogs of angular direction cosines differing from the voltage values by only a scaler factor.

The lag error η_A after a time interval t = T between the actual value of $c\ell$ or cm and the filter output is given by:

$$\eta_A = e_2(T) - e_1(T) = - E_1 e^{-\frac{T}{\tau}} \qquad \text{(B. 3)}$$

A plot of filter lag error η_A as a function of the filter time constant τ is shown in Fig. B. 4. A maximum initial offset (between received signal and ambient filter capacitor charge) of 180 degrees is assumed.* Integration time or sample time T is 0. 5 second.

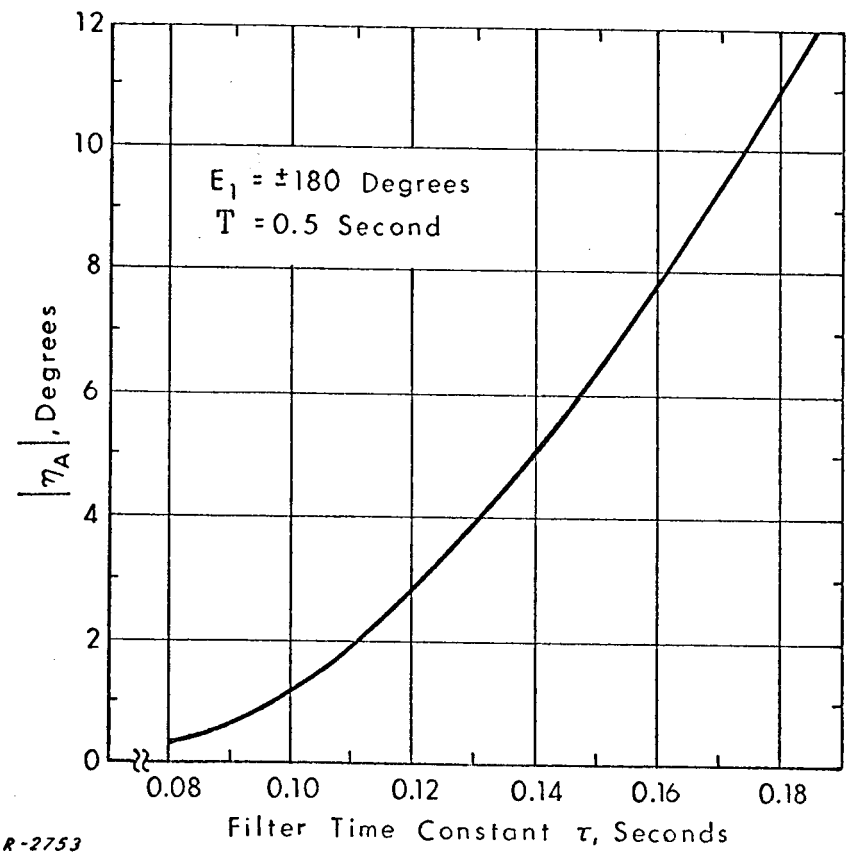

Fig. B. 4 $|\eta_A|$ as a Function of Filter Time Constant τ for a Sample Time T = 0. 5 Second.

*η_A is proportional to initial offsets less than 180 degrees.

B. 3 Error Due to Vehicle Dynamics

The maximum filter lag error due to vehicle dynamics is a function of the filter time constant and the maximum rate of change of $c\ell$ and cm. ω_{max} was calculated in Eq. (B. 1) to be approximately 6. 8 degrees per second. For simplicity this rate of change is assumed to be linear. Thus:

$$e_1(t) = 6.8\,t \qquad t \geq 0$$
$$= 0 \qquad t = 0 \qquad \text{(B. 4)}$$

For computational simplicity the assumption is also made that the initial capacitor charge is zero. Figure B. 5 shows the rate of change in $c\ell$ or cm, and the corresponding charge on the filter capacitor.*

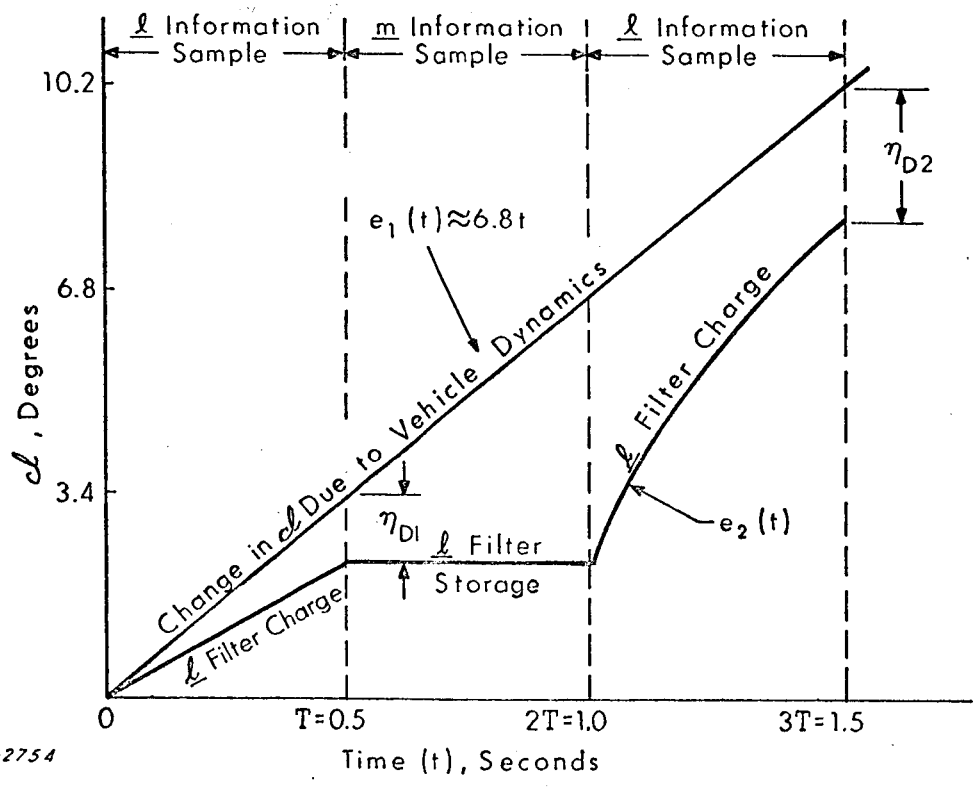

Fig. B. 5 ℓ Filter Capacitor Charge as a Function of a Change in cℓ

*Figure B. 5 shows the charge on the ℓ filter capacitor. An identical charge function exists for the m filter capacitor for a similar rate of change of cm.

The time constant τ of either filter shown in Fig. B. 2 is defined to be:

$$\tau = RC \tag{B. 5}$$

From the circuit of Fig. B. 2:

$$Z(s) = R + \frac{1}{sC} \tag{B. 6}$$

$$I(s) = \frac{E_1(s)}{R + \frac{1}{sC}} \tag{B. 7}$$

$$E_2(s) = \frac{I(s)}{sC} = \frac{E_1(s)}{s\tau + 1} \tag{B. 8}$$

The Laplace transform of Eq. (B. 4) is:

$$E_1(s) = \frac{6.8}{s^2} \tag{B. 9}$$

Therefore:

$$E_2(s) = \left[\frac{6.8}{\tau}\right]\left[\frac{1}{s^2(s + \frac{1}{\tau})}\right] \tag{B.10}$$

$$= 6.8\left[\frac{1}{s^2} - \frac{\tau}{s} + \frac{\tau}{s + \frac{1}{\tau}}\right] \tag{B.11}$$

Converting Eq. (B. 11) to the time domain:

$$e_2(t) = 6.8\left[t - \tau\left(1 - e^{\frac{-t}{\tau}}\right)\right] \tag{B.12}$$

The filter lag error η_{D1} due to vehicle dynamics is, at t = T second:

$$\eta_{D1} = e_1(T) - e_2(T) \tag{B.13}$$

$$= 6.8\tau\left(e^{\frac{-0.5}{\tau}} - 1\right) \quad \text{for } T = 0.5 \tag{B.14}$$

At $t = 2T$, when the filter again starts to charge, there is an initial charge of $(6.8T - \eta_{D1})$ on the filter capacitor.

To solve for the filter output $e_2(t)$ in the interval $2T < t \leq 3T$ we have the initial condition

$$e_2(2T) = 6.8T - \eta_{D1} \tag{B.15}$$

and the input $e_1'(t')$ for the corresponding interval is (see Fig. B.5)

$$\begin{aligned} e_1'(t') &= 6.8(t' + 2T) \qquad t' > 0 \\ &= 0 \qquad\qquad\quad t' \leq 0 \end{aligned} \tag{B.16}$$

where $t' = (t - 2T)$. The resulting output $e_2(t)$ is thus being obtained by computing the response of the filter to the input given by Eq. (B.16) and the initial capacitor charge of (B.15). The response $e_2'(t')$ to the above conditions is given as the inverse transform of

$$\mathcal{L}\left[e_2'(t')\right] = 6.8\left\{\frac{1}{s^2} + \frac{2T}{s}\right\}\frac{1}{s\tau + 1} + (6.8T - \eta_{D1})\frac{1}{s\tau + 1} \tag{B.17}$$

where the effect of the initial condition on the filter capacitor is included as an impulse input occurring at $t' = 0$. The inverse transform of Eq. (B.17) is

$$\begin{aligned} e_2'(t') &= 6.8\left[t' - \tau\,(1 - e^{-t'/\tau})\right] + 13.6\,T(1 - e^{-t'/\tau}) \\ &\quad + (6.8T - \eta_{D1})\,e^{-t'/\tau} \\ &= 6.8t' + 13.6T - 6.8\tau(1 - e^{-t'/\tau}) - (6.8T + \eta_{D1})\,e^{-t'/\tau} \end{aligned} \tag{B.18}$$

The total error η_{D2} is then

$$\eta_{D2} = e_1(3T) - e_2'(T) = e_1(3T) - e_2(3T) \qquad \text{(B. 19)}$$

$$= (1 - e^{-T/\tau})\, \eta_{D1} - 6.8T\, e^{-T/\tau}$$

$$= -\frac{\eta_{D1}^{\,2}}{6.8\tau} - 6.8T\, e^{-T/\tau} \qquad \text{(B. 20)}$$

Both these error coefficients $|\eta_{D1}|$ and $|\eta_{D2}|$ are plotted in Fig. B. 6 as a function of τ.

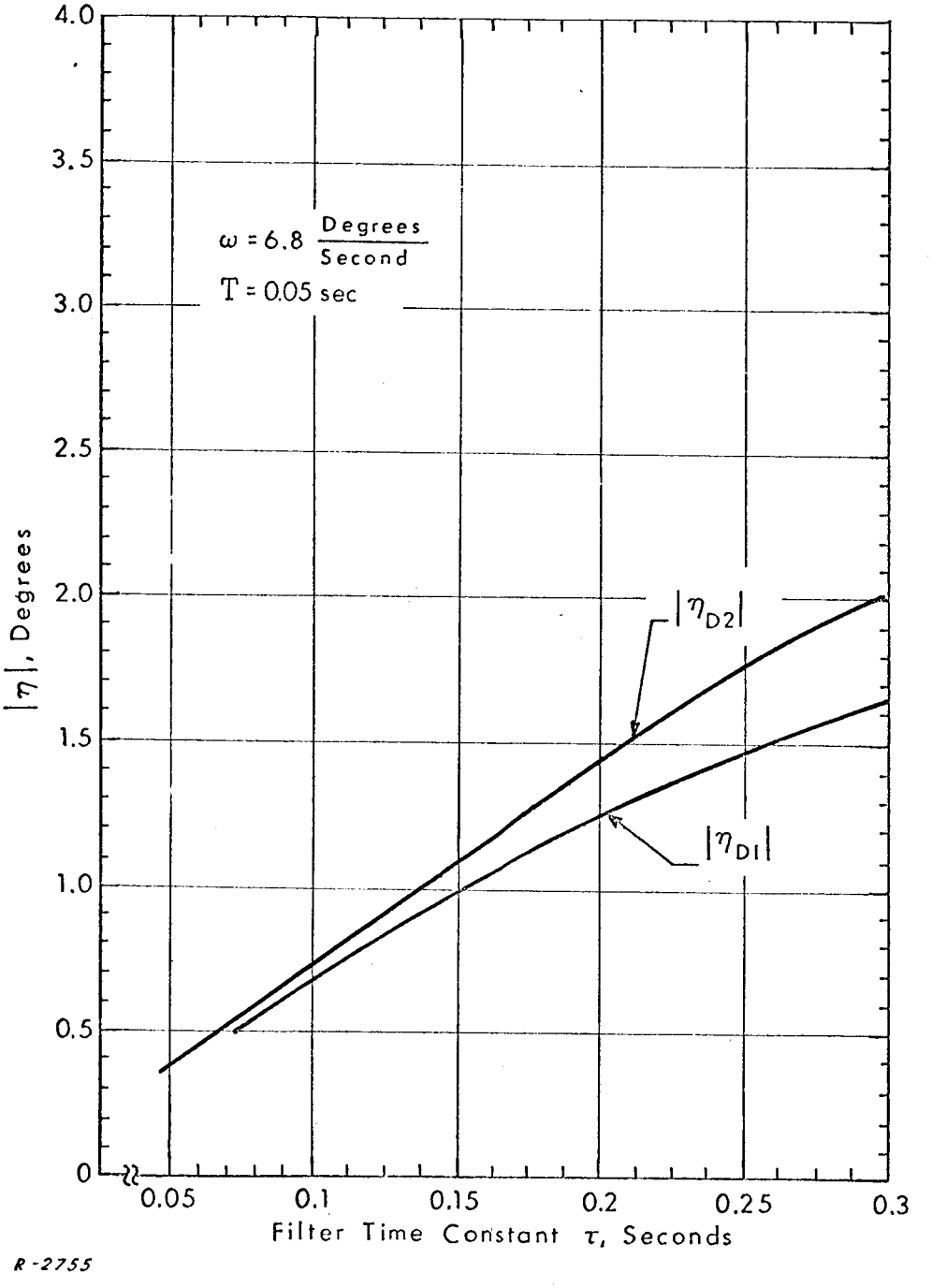

Fig. B. 6 Filter Lag Error η due to Vehicle Dynamics-Plotted as a Function of Filter Time Constant τ.